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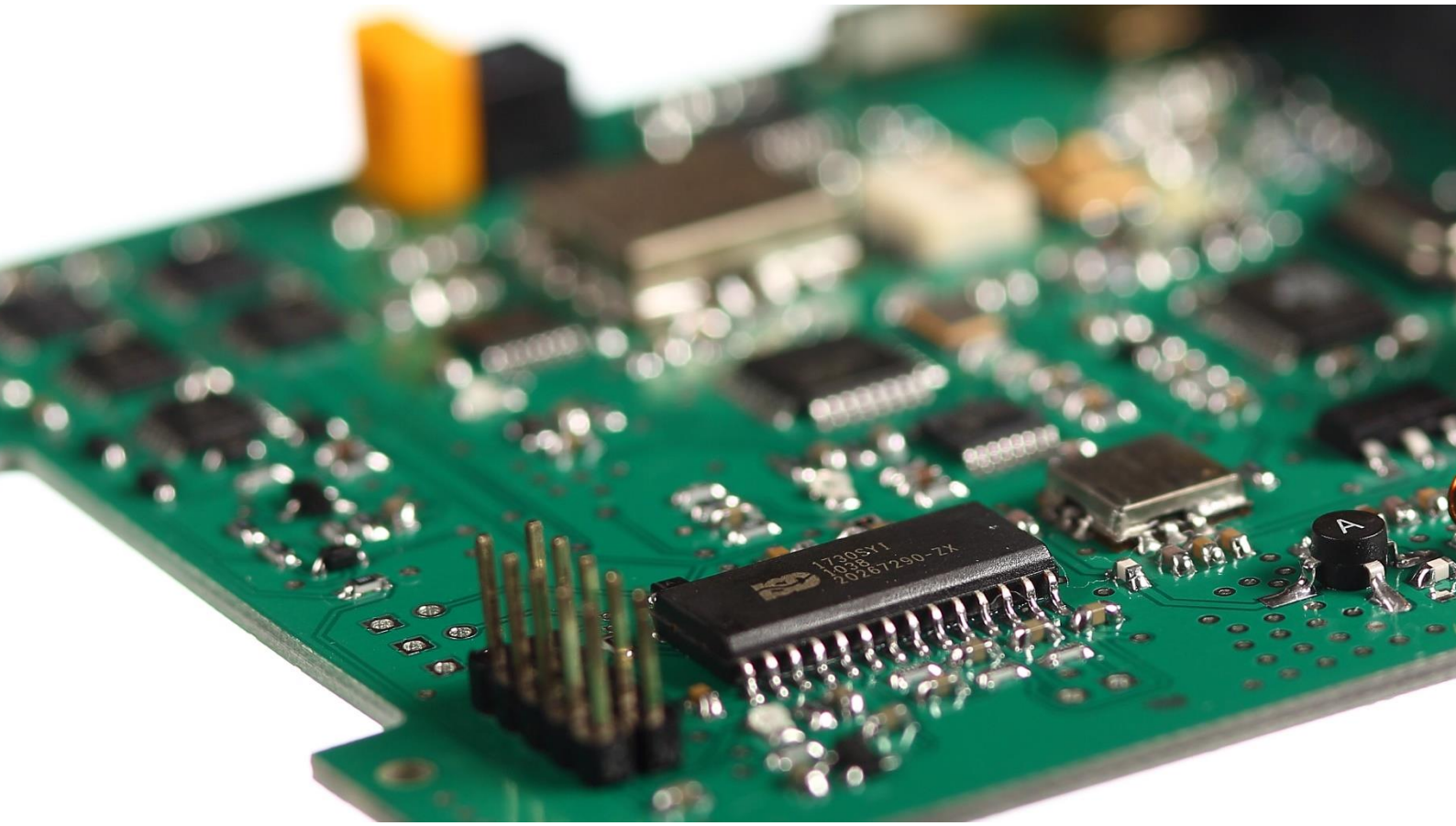
Prepared: **Julija Volkova, CAD/Technical Documentation Engineer**
Revised: **Erikas Kneižys, CINO**
Approved: **Ernestas Kalabuckas, CTO**

M6P Platform/Payload Interface Control Document



Point of Contact: **Vytenis Buzas, CEO**
Address: **Mokslininku str. 2A, LT-08412 Vilnius, Lithuania**
Mobile: **+370 663 53355**
E-mail: **vytenis@n-avionics.com**

Contents

1 Mechanical Interfaces

M6P provides 4U volume available for the Payload. Figure 1 below represents the structure of the Platform where 2U volume at the –Z side including “tuna cans” are secured for the CubeSat avionics (1).

The Payload interface board (2) accommodates Platform/Payload connectors which contain electrical and data interfaces for the Payload.

The main Payload mounting option for the “ride sharing” clients is a modular PC/104 standard stacking into the stack rings (3). The stack can be facing X, Y or Z directions as required, and the length of the stack can be increased or decreased if needed. Stack ring mechanical drawing is given in Appendix 3. Stacking Ring Mechanical Drawing. Figure 1 shows 2 x 1U plus 1 x 2U configuration. Payload envelope dimensions in mm and arrangement of the Platform axes are given in Figure 2 and Figure 3 below.

Another (Single Payload) option of Payload mounting is fixing it directly to the frame without the use of stack mounting rings, as explained in sections 1.4, 1.5, 1.6 , 1.7.

Please note that the mechanical drawings provided in this document are for initial information on Payload mounting. STEP files will be provided for detailed representation for available integration options.

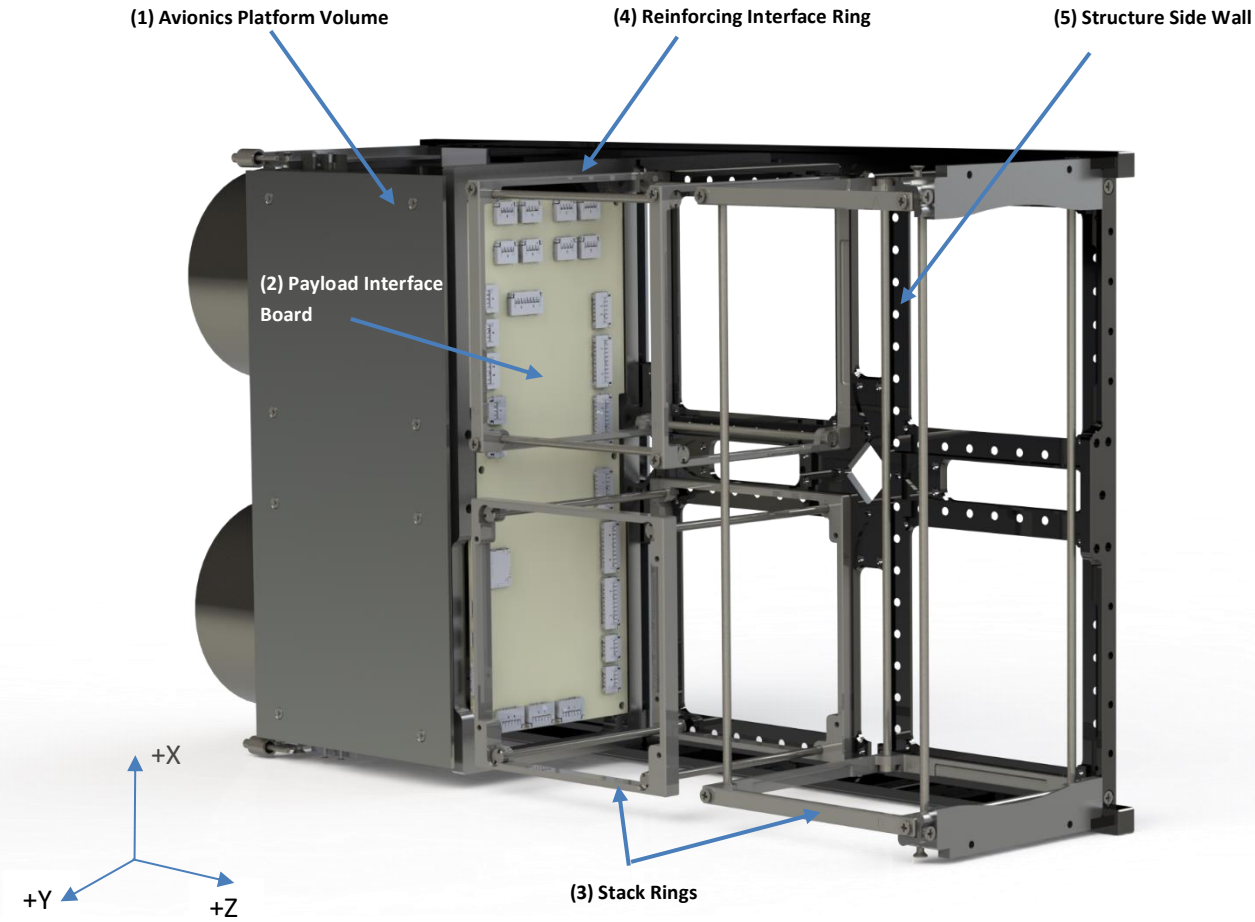


Figure 1. 6U Platform structure representation

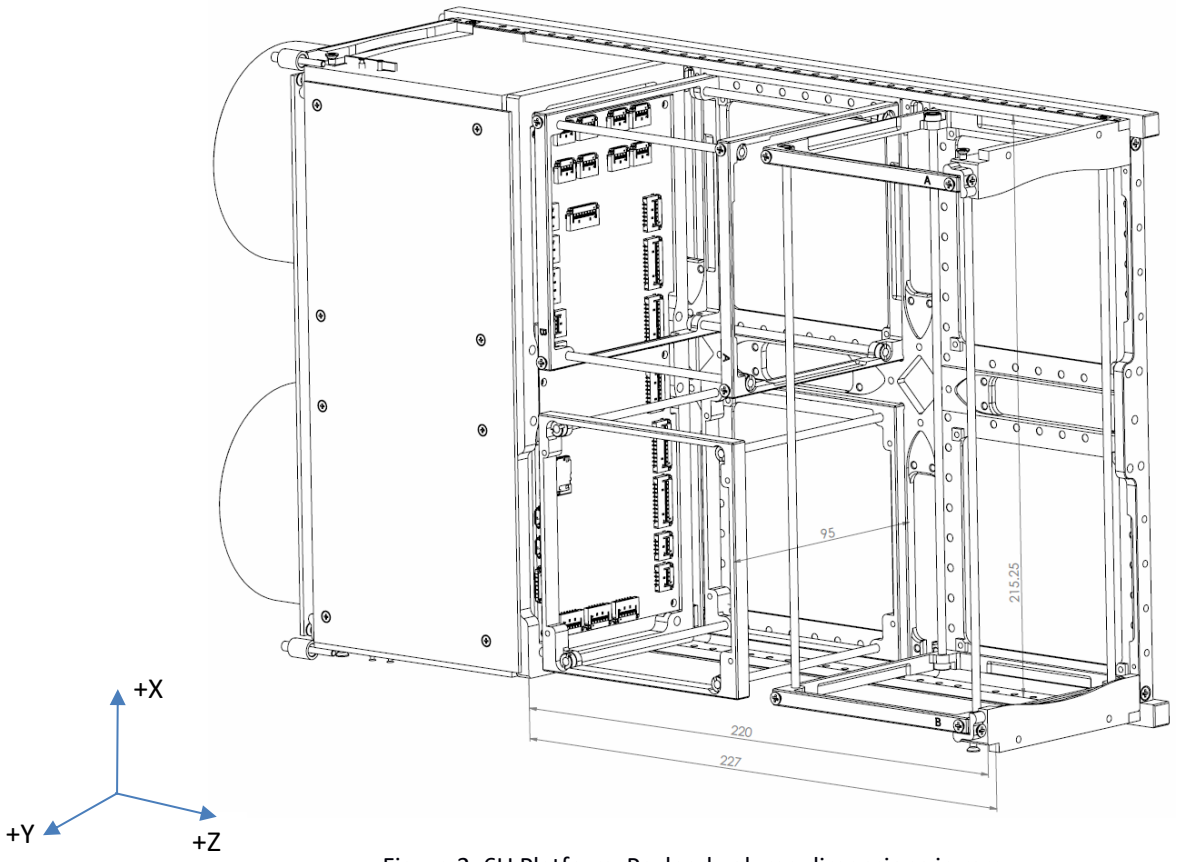


Figure 2. 6U Platform, Payload volume dimensions in mm

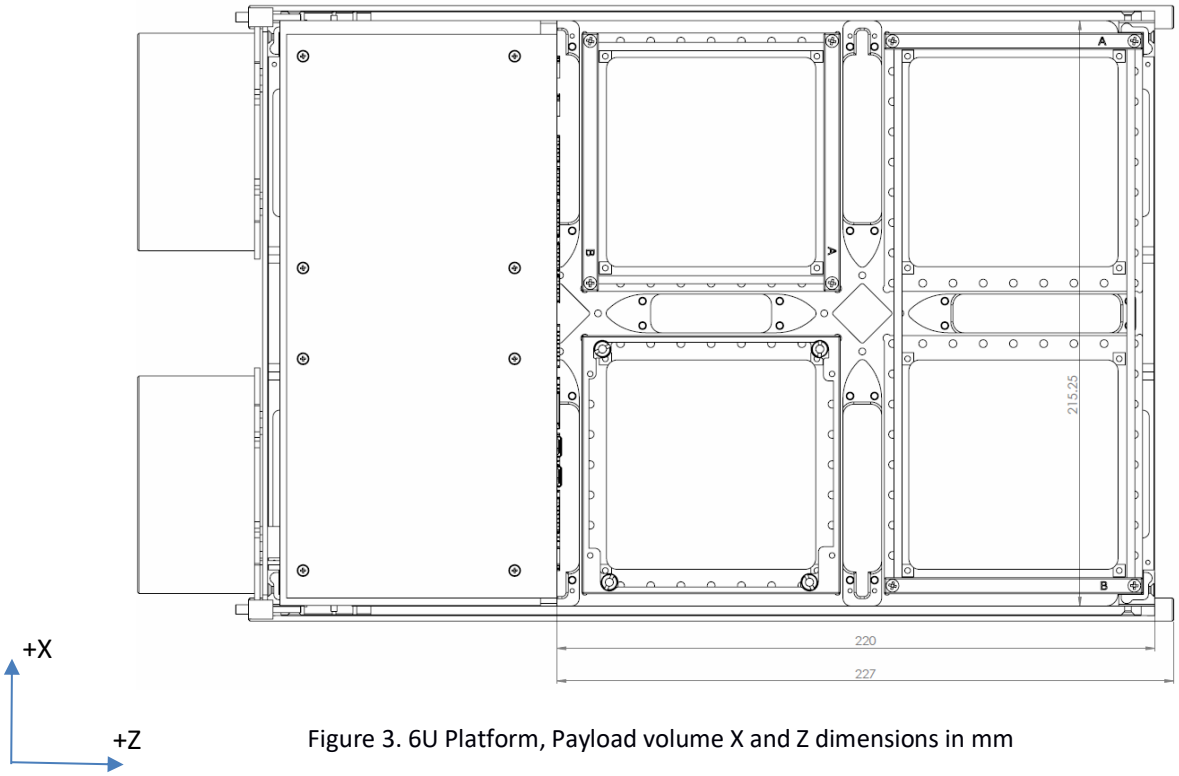


Figure 3. 6U Platform, Payload volume X and Z dimensions in mm

1.1 Deployables

Any deployable parts of the Payload must fit through the openings in the structure in the directions of +Y/-Y as a standard option. Structure +Y/-Y face openings and their dimensions are shown in Appendix 1. +Y/-Y Side Structure Mechanical Interface. Exposing the Payload through +X/-X and +Z faces are also considerable as additional options agreed with the client.

1.2 Side Wall Protrusions

The +Y/-Y, +X/-X faces have a clearance of 12mm above the rails and the +Z face has a clearance of 4.5 mm (refer to Astrofein deployer requirements) above the rail ends. A safety margin of 2mm needs to be taken into account due to vibrations during the launch.

1.3 Stacking Ring Mechanical Interface

PC/104 form factor complying stacking rings are available for payload mounting. Any of the Payload components can be assembled into a stack using two separate stack rings A and B, four threaded M3 stainless steel rods and the stack is secured with dedicated nuts at each side. Stack ring set can be oriented in X, Y or Z directions. Stack ring A mechanical dimensions are given in Appendix 3. Stacking Ring Mechanical Drawing.
Please note that stack rings A and B are mirrored, because stack holes have no axes of symmetry.

1.4 +Y/-Y Side Interface

The mechanical drawing of +Y/-Y face of the structure is given in Appendix 1. +Y/-Y Side Structure Mechanical Interface. +Y and –Y structure faces have 128 M2.5 countersink clearance holes on each side available for Payload. In addition, 46 threaded M2 and 5 threaded M2.5 holes are present on the structure wall and can be used if needed. The side wall of the frame is symmetrical along the X and Z axes. There are six equal major 77 x 77mm openings in the frame wall on Y/-Y sides each, four of which are available for the Payload.

1.5 +X/-X Side Interface

The mechanical drawing of +X/-X face of the structure is given in Appendix 2. +X/-X Side Structure Mechanical Interface. +X and –X sides have 46 threaded M2.5 holes each, available on the Payload side.

1.6 +Z Side Interface

The mechanical drawing of +Z face of the structure is given in Appendix 4. +Z/-Z Side Structure Mechanical Interface. +Z face has 20 threaded M2.5 and 10 threaded M3 holes available for the Payload mounting.

1.7 Payload/Platform Junction Reinforcing Ring Interface

Additional reinforcing ring is present at the Platform/Payload interface and can be used for Payload mounting, shown in Appendix 5. Reinforcing Interface Ring Mechanical Drawing. This ring has eight M3 clearance holes. 4 holes at +X side and 4 at –X side are conforming to the PC/104 standard and can be utilized for Payload mounting if needed.

2 Electrical Interface

2.1 Pinout

All connectors (4, 6, 8, 10 pins) are Molex Pico-Lock series. The receptacle part numbers are 504051-0401, 504051-0601, 504051-0801 and 504051-1001. Electrical connectors are depicted in Figure 4.

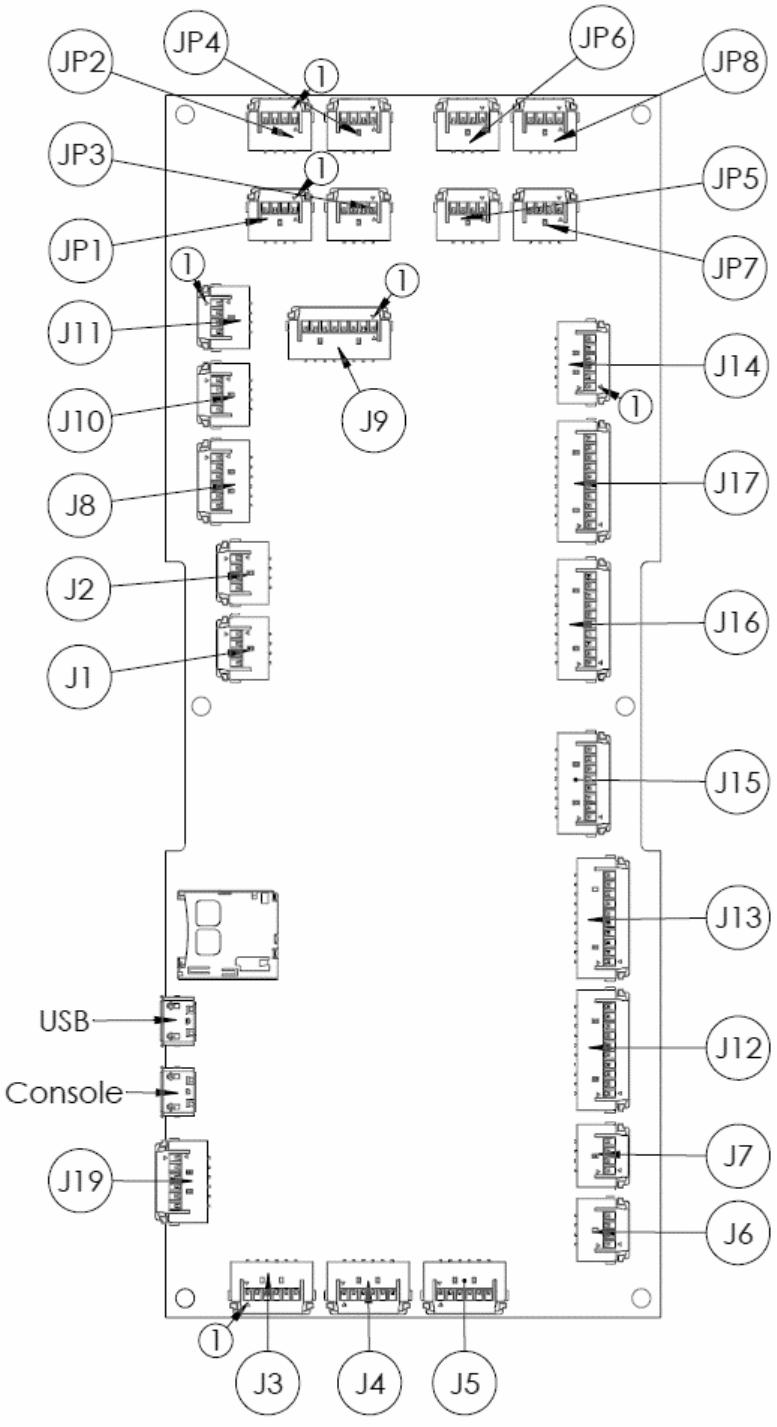


Figure 4. Electrical connectors legend

2.1.1 CAN

Table 1. CAN interface pinout

	J1	J2
	CAN2	**CAN2**
1	CAN2-L	CAN2-L
2	CAN2-L	CAN2-L
3	CAN2-H	CAN2-H
4	CAN2-H	CAN2-H

2.1.2 SPI/I2C

SPI interface signals are 3.3 V TTL level. I2C interfaces are pulled-up with 2.2 kΩ resistors to 3.3 V on the Payload controller board.

Table 2. SPI and I2C interfaces pinout

	J3	J4	J5
	SPI2 (buffered)	**SPI4 (buffered)**	**SPI5 (buffered)**
1	GND	GND	GND
2	SPI2_Buffer_Enable (H = Enabled)	SPI4_Buffer_Enable (H = Enabled)	SPI5_Buffer_Enable (H = Enabled)
3	SPI2_MISO (PI2)	SPI4_MISO (PE5)	SPI5_MISO (PJ11)
4	SPI2_MOSI (PI3)	SPI4_MOSI (PE6)	SPI5_MOSI (PJ10)
5	SPI2_SCK (PI1)	SPI4_SCK (PE2)	SPI5_SCK (PK0)
6	SPI2_NSS (PI0)	SPI4_NSS (PE4)	SPI5_NSS (PH5)
	J6	**J7**	
	I2C1	**I2C2**	
1	GND	GND	
2	I2C1_SCL (PB8)	I2C2_SCL (PH4)	
3	I2C1_SDA (PB9)	I2C2_SDA (PH5)	
4	GND	GND	

2.1.3 UART/USART/RS422

UART/USART interface signals are 3.3 V TTL level.

Table 3. UART, USART and RS422 interfaces pinout

	J8	J9
	UART5 (buffered)	**USART6 (buffered)**
1	GND	GND
2	UART5_Buffer_Enable (H = Enabled)	USART6_Buffer_Enable (H = Enabled)
3	UART5_TX (PC12)	USART6_RX (PC7)
4	UART5_RX (PD2)	USART6_TX (PC6)
5	UART5_RTS (PC8)	USART6_RTS (PG8)
6	UART5_CTS (PC9)	USART6_CTS (PG13)
7		USART6_CK (PG7)
8		GND
	J10	**J11**
	RS422 (UART7)	**RS422 (UART8)**
1	TX+	TX+
2	TX-	TX-
3	RX+	RX+
4	RX-	RX-

2.1.4 ADC

ADC signal ranges from 0 to 3.3 V with a frequency range up to 10 kHz.

Table 4. ADC connector pinout

	J12	J13
	ADC inputs / GPIO - 1	**ADC inputs / GPIO - 1 / PPS**
1	GND	GND
2	ADC1_IN16 (PA0)	ADC1/2/3_IN10 (PC0)
3	ADC1_IN17 (PA1)	ADC1/2/3_IN11 (PC1)
4	ADC1/2_IN14 (PA2)	ADC3_IN0 (PC2_C)
5	ADC1/2_IN15 (PA3)	ADC3_IN1 (PC3_C)
6	ADC1/2_IN9 (PB0)	ADC1/2_IN4 (PC4)
7	ADC1/2_IN5 (PB1)	ADC1/2_IN8 (PC5)
8	ADC3_IN6 (PF10)	GND
9	ADC1_IN2 (PF11)	GPS_PPS
10	GND	GPS_PPS

2.1.5 H-bridge/PWM/GPIO

PWM/GPIO signals are 3.3 V TTL level. H-bridge (J14) outputs are 3.3 V, PWM controlled, up to 1.0 A total current (all three outputs).

Table 5. H-bridge, PWM and GPIO connector pinout

	J14	J15
	H-bridges	**PWM outputs (buffered)**
1	Hbridge1-P (driven from TIM8_CH1)	GND
2	Hbridge1-N (driven from TIM8_CH1)	PWM channels Buffer Enable (H = Enabled)
3	Hbridge2-P (driven from TIM8_CH2)	TIM12_CH1 (PH6)
4	Hbridge2-N (driven from TIM8_CH2)	TIM12_CH2 (PH9)
5	Hbridge3-P (driven from TIM8_CH3)	TIM4_CH2 (PD13)
6	Hbridge3-N (driven from TIM8_CH3)	TIM5_CH1 (PH10)
7		TIM5_CH2 (PH11)
8		TIM5_CH3 (PH12)
	J16	**J17**
	GPIO - PI (Buffered with Auto direction)	**GPIO - PJ (Buffered with Auto direction)**
1	GND	GND
2	GPIO PI Buffer Enable (H = Enabled)	GPIO PJ Buffer Enable (H = Enabled)
3	PI4	PJ0
4	PI8	PJ1
5	PI10	PJ2
6	PI11	PJ3
7	PI12	PJ12
8	PI13	PJ13
9	PI14	PJ14
10	PI15	PJ15

2.1.6 Power Outputs

Four EPS channels are available for the Payload and each channel can be configured to 3.3, 5, 12 or 15 V or V_{bat} (6.4-8.4 V), with a current rating up to 3.0 A (depending on output voltage and final Payload configuration).

Table 6. Power connector pinout

	JP1	JP2	JP3	JP4
	Power out channel 1	**Power out channel 1**	**Power out channel 2**	**Power out channel 2**
1	GND	GND	GND	GND
2	GND	GND	GND	GND
3	Power Supply Channel 1	Power Supply Channel 1	Power Supply Channel 2	Power Supply Channel 2
4	Power Supply Channel 1	Power Supply Channel 1	Power Supply Channel 2	Power Supply Channel 2
	JP5	**JP6**	**JP7**	**JP8**
	Power out channel 3	**Power out channel 3**	**Power out channel 4**	**Power out channel 4**
1	GND	GND	GND	GND
2	GND	GND	GND	GND
3	Power Supply Channel 3	Power Supply Channel 3	Power Supply Channel 4	Power Supply Channel 4
4	Power Supply Channel 3	Power Supply Channel 3	Power Supply Channel 4	Power Supply Channel 4

3 Data Interfaces

Communication between the Platform and Payload is being implemented using CubeSat Space Protocol (CSP), an efficient open-source protocol stack developed specifically for network-centric nanosatellite systems. Due to the use of this protocol, it is required that the CSP implementation is supported by the Payload. Architecture diagram can be seen in Figure 8.

Payload CSP ID values range from 12 to 15. A full list of all M6P network node CSP IDs can be found in a separate document when required. Payload is integrated into the main M6P network through the Payload controller (PC) and has the ability to communicate with all other subsystems of the Platform directly. Request-reply pattern is used for all communications, and unsolicited messages are not allowed.

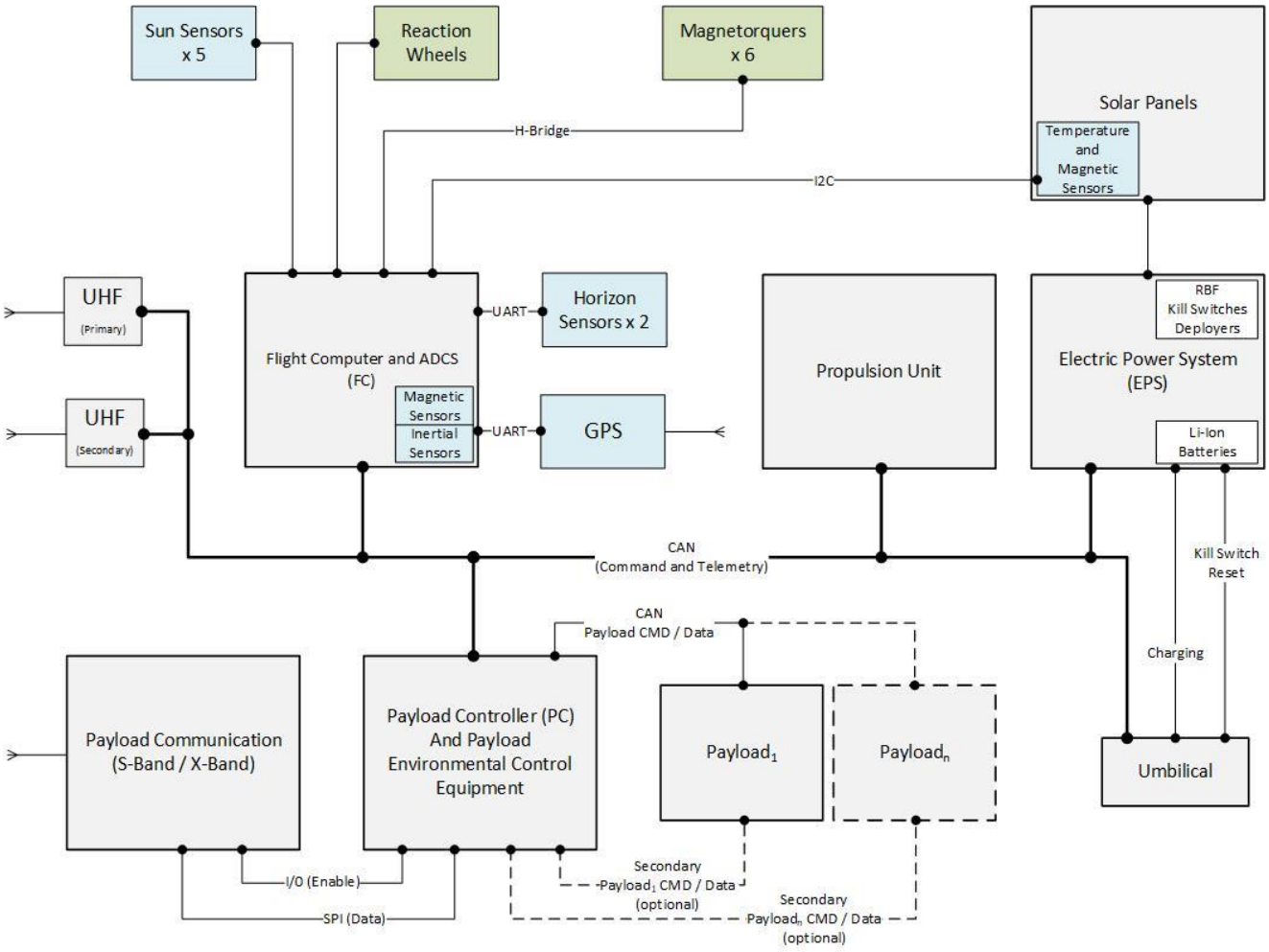


Figure 5. M6P Architecture diagram (it might vary according to the final Client's requirements)

Detailed information about M6P Software ICD can be found in the following documents:

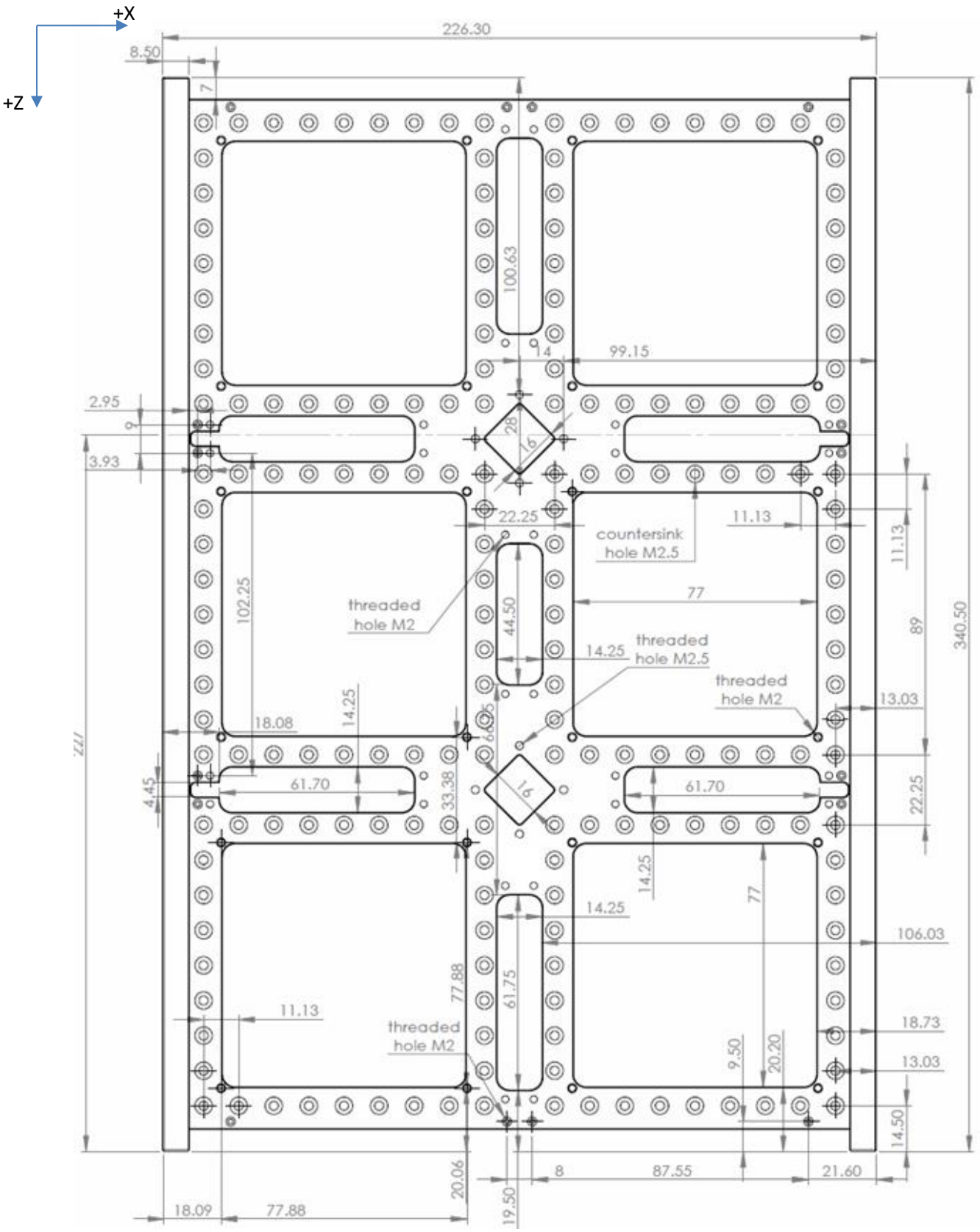
- *M6P Platform Rideshare Software Interface Control Document;*
- *M6P Platform Software Interface Control Document;*

4 Thermal Interface

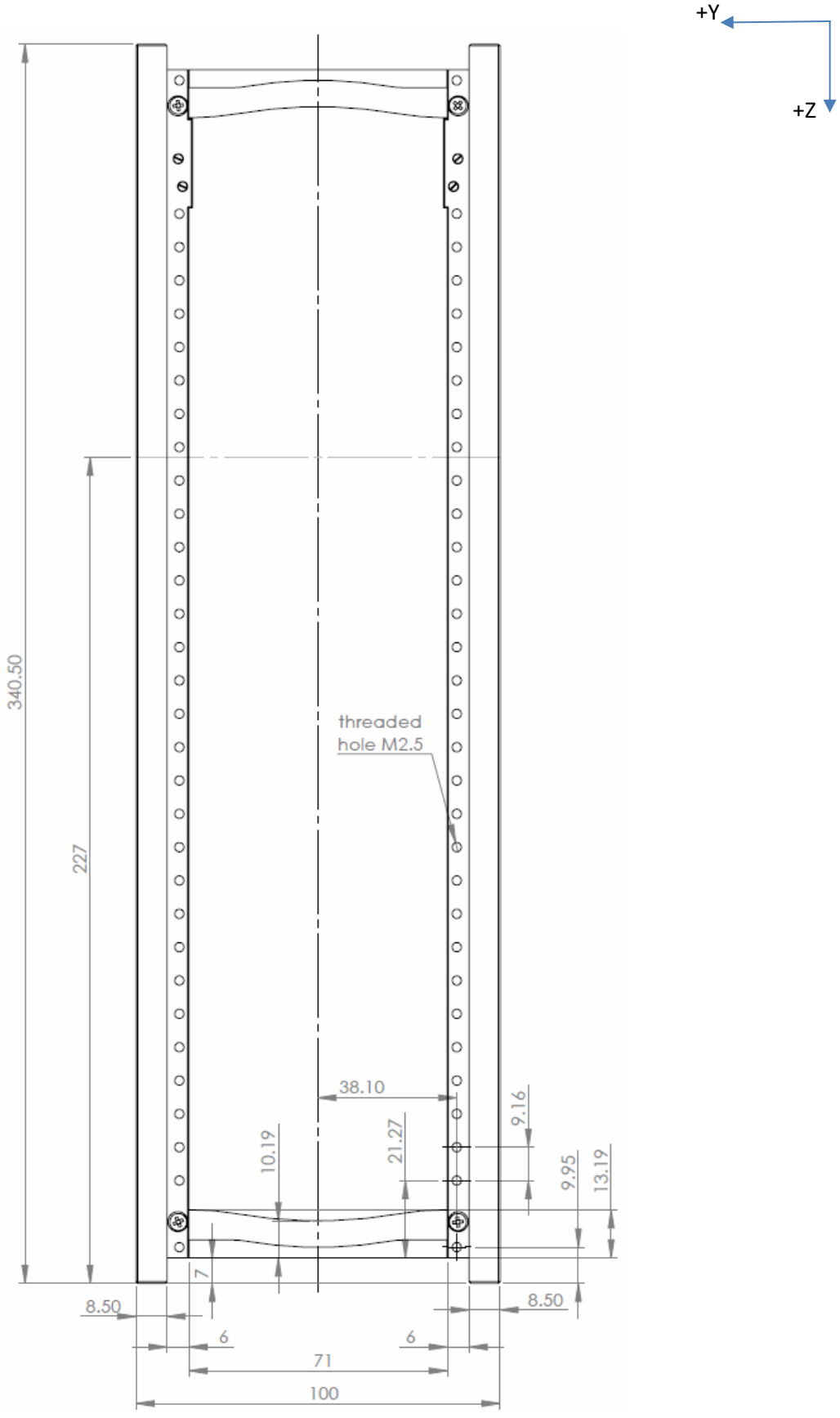
Due to the variety of Payloads provided by different customers, NanoAvionics does not provide a standardized thermal interface description. Final thermal harness, if needed, and thermal interfacing specifics depend on several parameters, such as but not limited to Payload power consumption, Payload efficiency, duty cycle per orbit, and maximum Payload temperature.

To ensure the highest Payload control reliability and efficiency, thermal interface analysis is carried out for each specified mission/Payload, which includes thermal calculations and simulations using CAD/FEM tools such as SolidWorks and MATLAB, including related sets of libraries. This method was adopted in order to best meet customer requirements with the highest possible attention to detail and analysis accuracy. This approach helps NanoAvionics to ensure each customer is provided with reliable Payload operating conditions throughout each mission's lifetime.

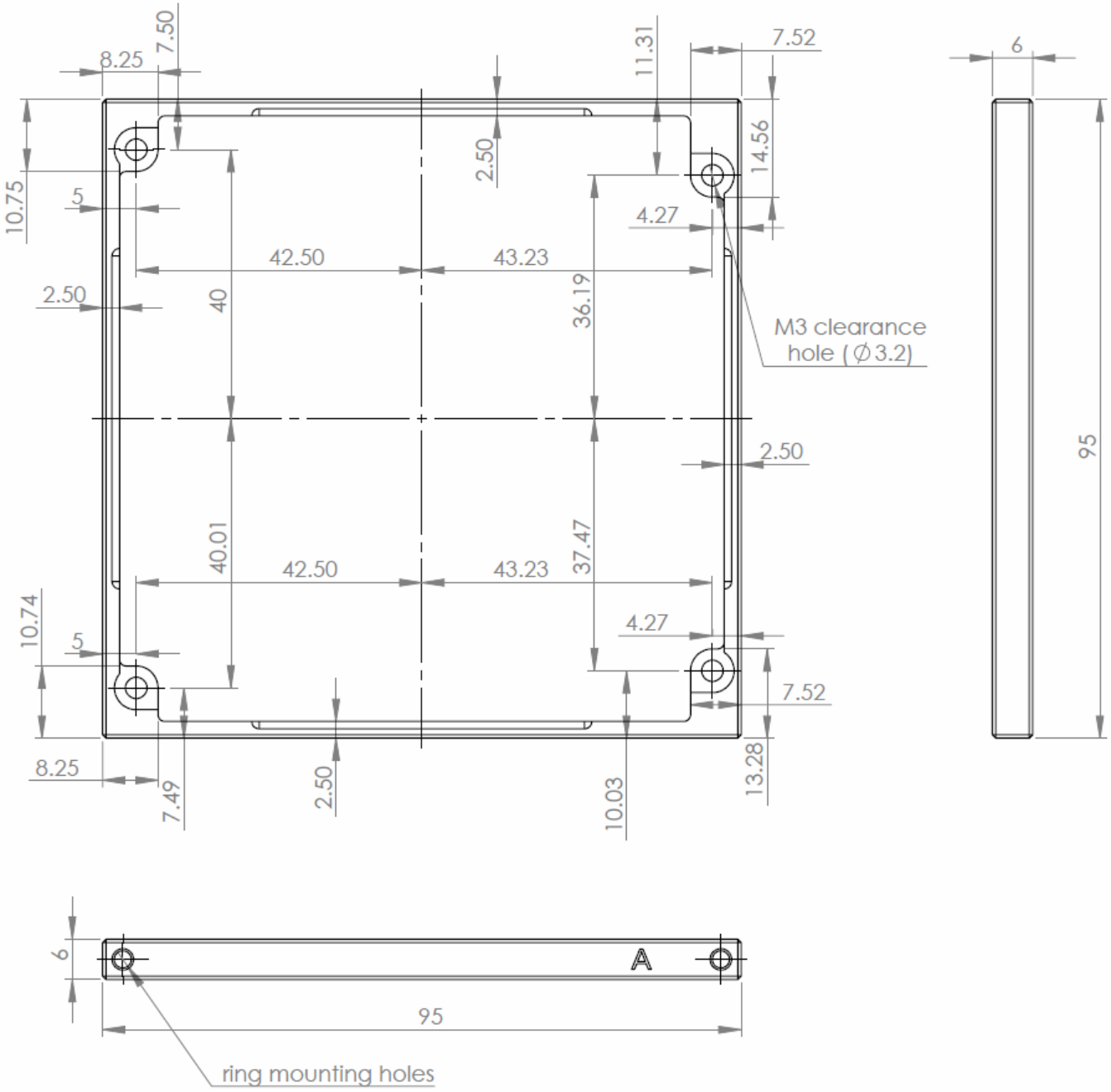
Appendix 1. +Y/-Y Side Structure Mechanical Interface



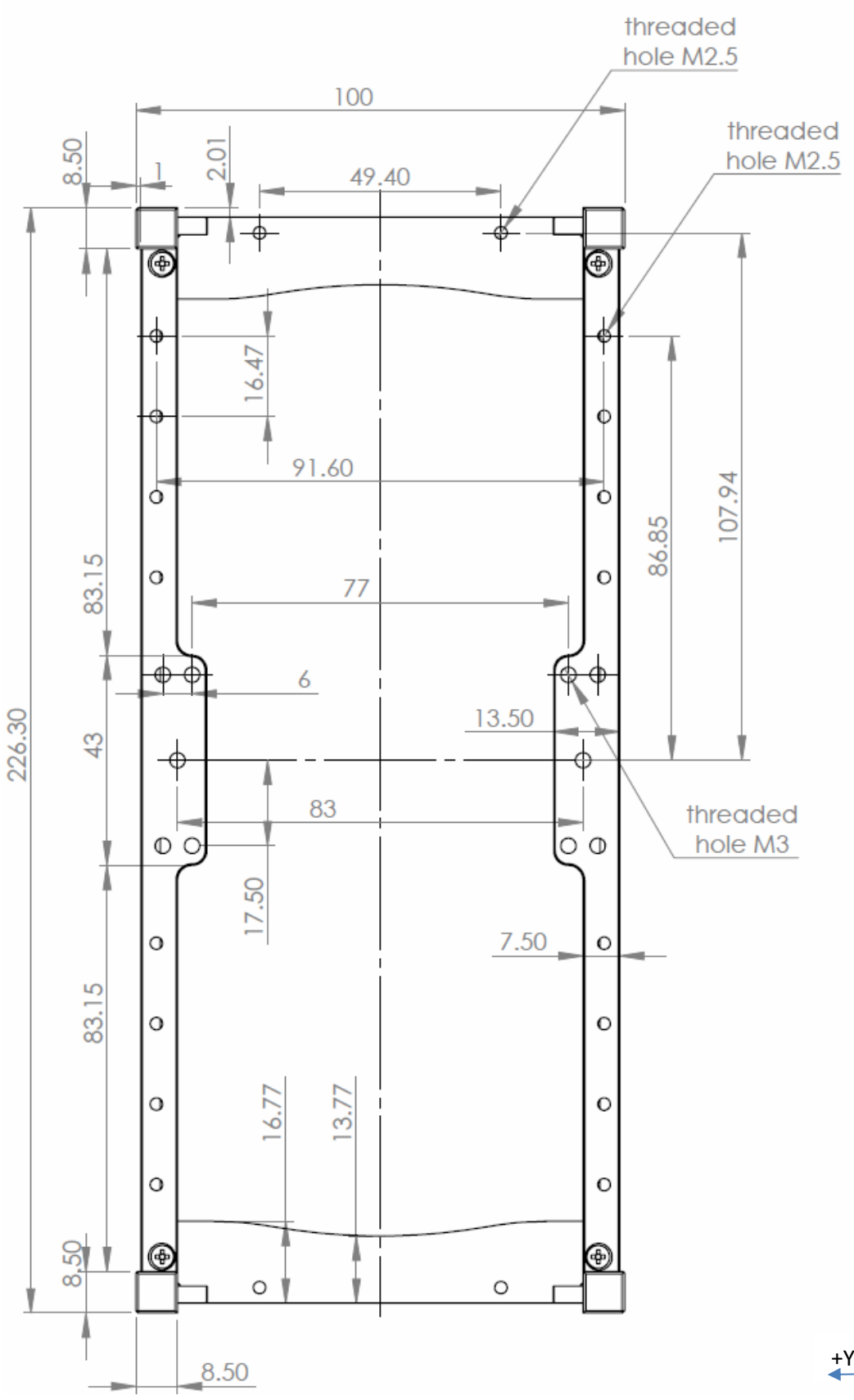
Appendix 2. +X/-X Side Structure Mechanical Interface



Appendix 3. Stacking Ring Mechanical Drawing



Appendix 4. +Z/-Z Side Structure Mechanical Interface



Appendix 5. Reinforcing Interface Ring Mechanical Drawing