

▲ With the industrial version of the PicoZed Board this design is rated for -40 to 85 degrees celsius

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▲ The camera can be powered by any power supply capable of delivering 4.5V - 14.5V at 6A

▲ CARRIER\_SRST# resets the processor as well as erases all debug configurations, memory content within the PS and PL.

▲ To shut down power to the PicoZed, PWR\_ENABLE and VCCIO\_EN should be pulled low.

VCCIO\_EN should be pulled low first to maintain proper shutdown sequencing.

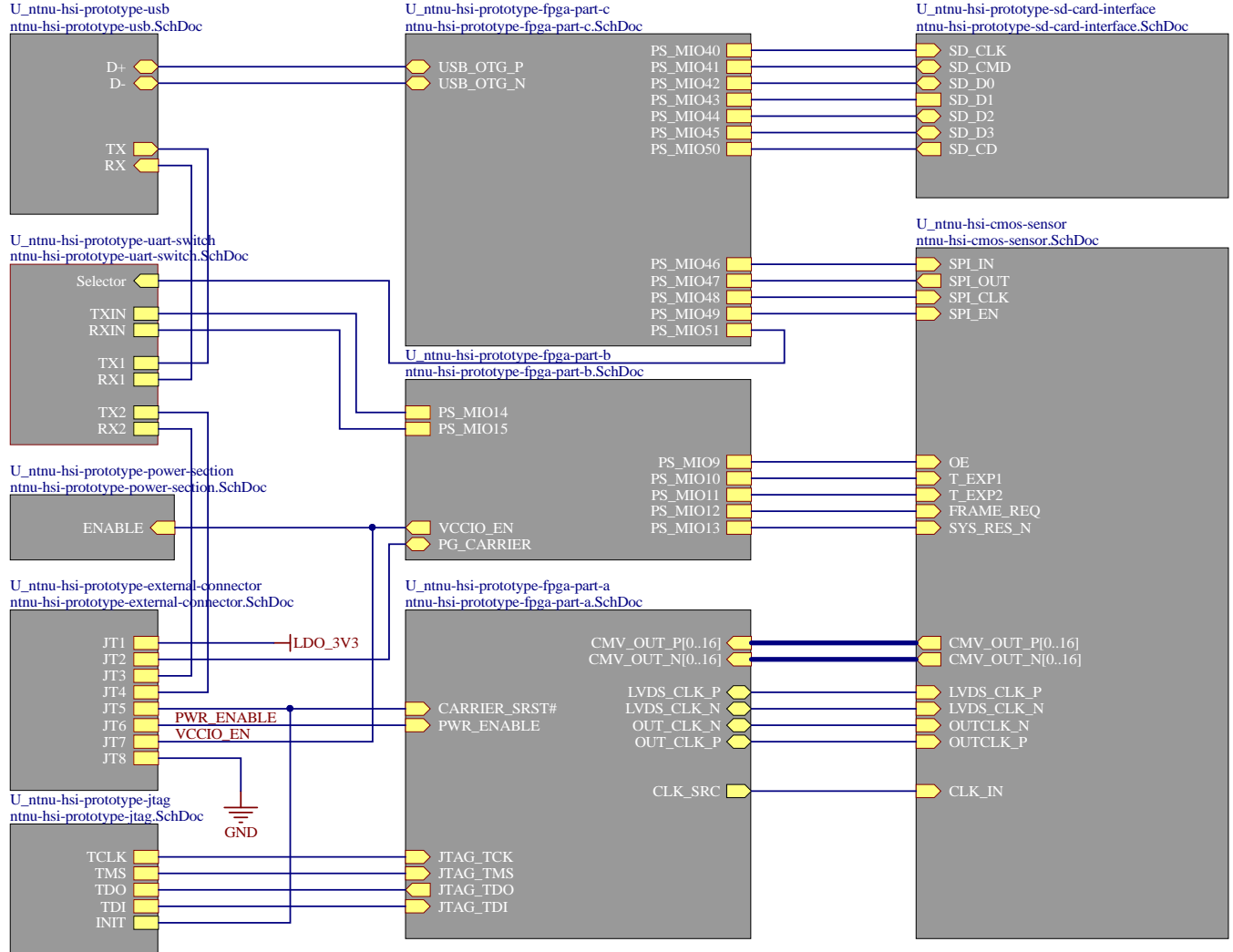
PWN\_ENABLE is tied to VIN on the card

▲ FPGA Bank 34 and 35 operate at 1.8V only because they are high-performance banks.

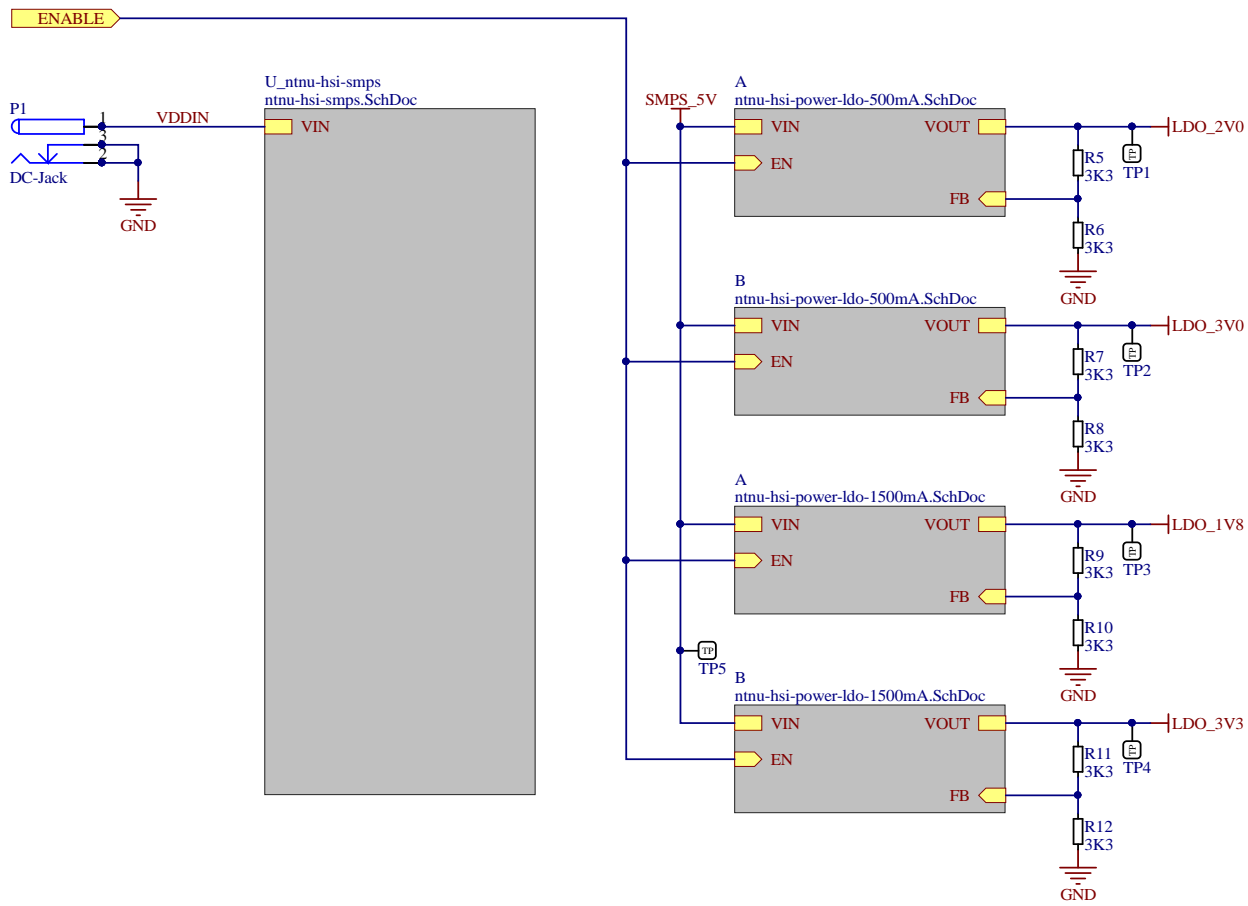
Bank 13 can be 3.3V

MIO0-MIO15 powered by 3.3V  
MIO30-MIO51 powered by 1.8V

▲ PG\_MODULE - External power-on reset signal. Resets the entire chip



	Title: Architecture Overview		
	Project:	HSI Prototype	Engineer: Julian V.
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Power supply sequencing is done on the PicoZed board and is not necessary for the bank/camera power supplies.



Title:	Main Power Section	
Project:	HSI Prototype	Engineer: Julian V.
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$V_{out} = 5V$   
 $R_{set} = 196\Omega$   
 $R_t = 86.6k\Omega$   
 Switching frequency  $f_{sw} = 780kHz$

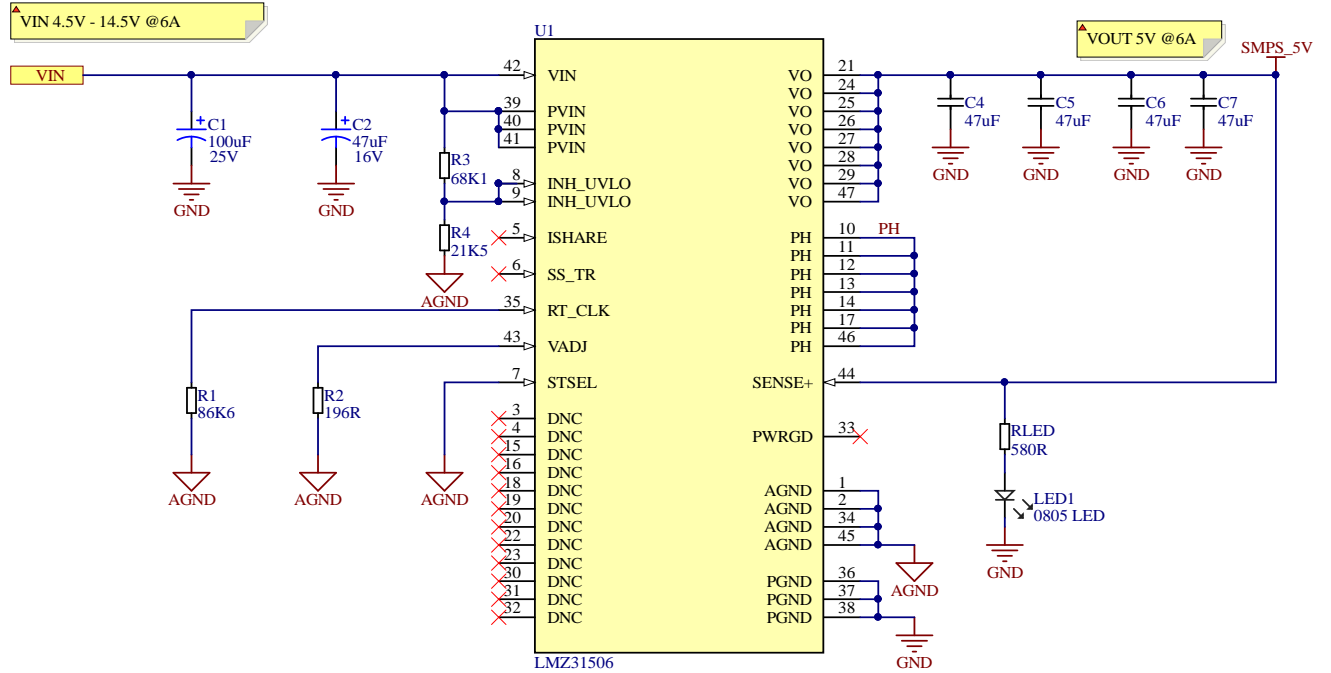
Undervoltage lockout at 5V:

$R_{uv1} = 68.1k\Omega$   
 $R_{uv2} = 21.5k\Omega$

UVL Hysteresis: 400mV

$T525D476M016ATE035$  16V 47uF  
 $T521D107M025ATE040$  25V 100uF

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time.



	Title:	Switch Mode Power Supply	
	Project:	HSI Prototype	Engineer: Julian V.
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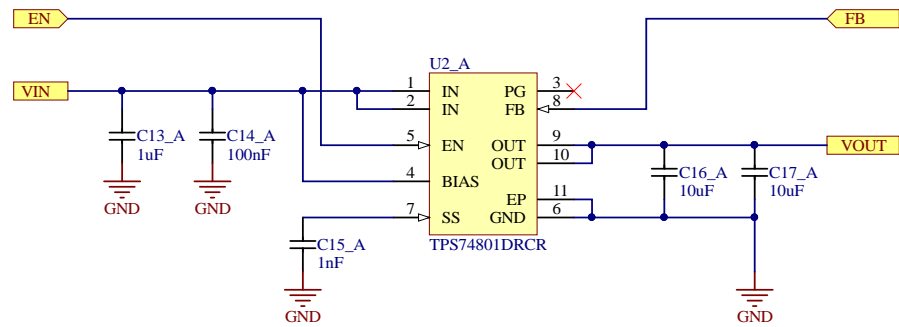
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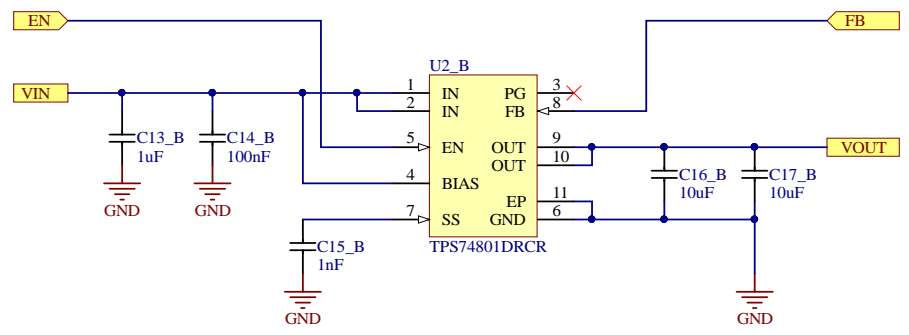
	Title: 1500mA Adjustable LDO	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
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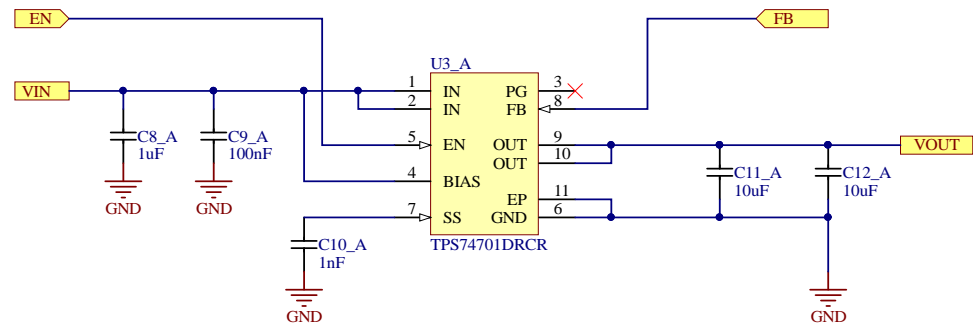
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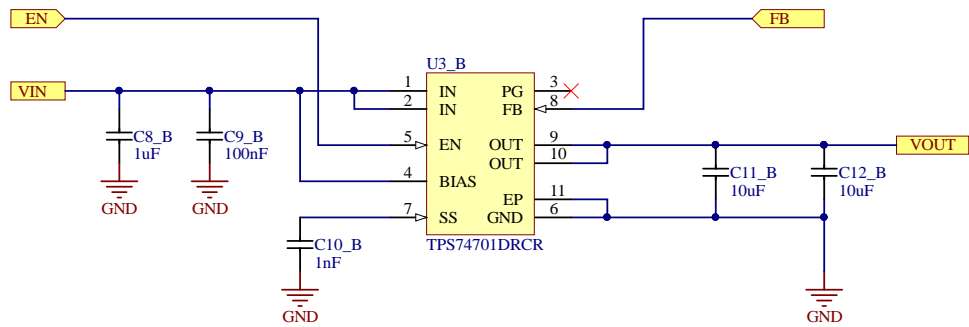
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	Title: 1500mA Adjustable LDO	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
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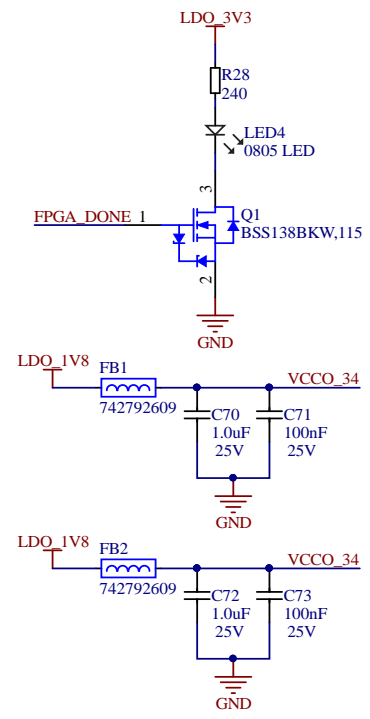
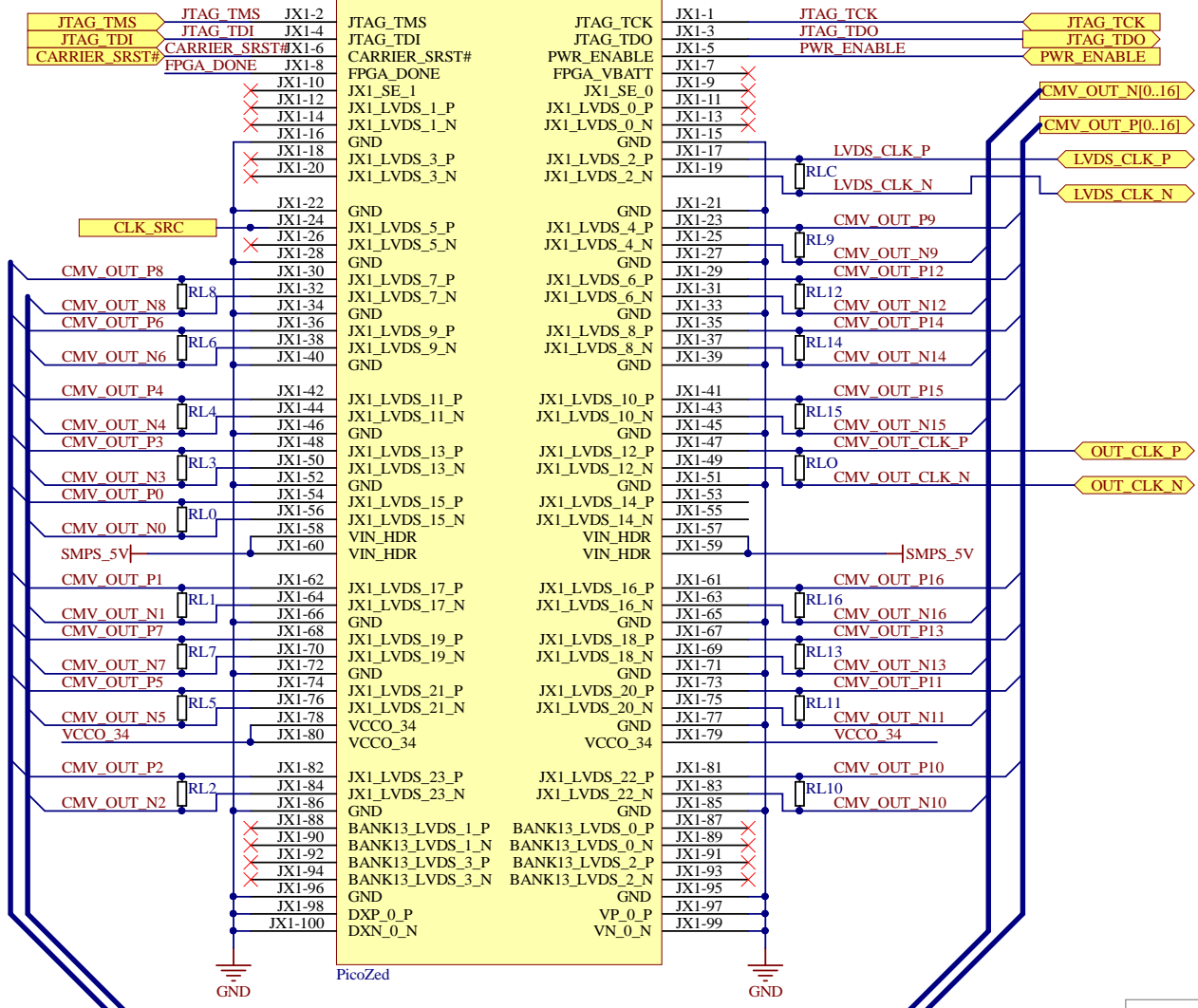
	Title: 500mA Adjustable LDO	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
	Revision: 1.0	Sheet: 5 of 15



	Title: 500mA Adjustable LDO	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
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# ZYNQ BANK 34/35

SOM4A

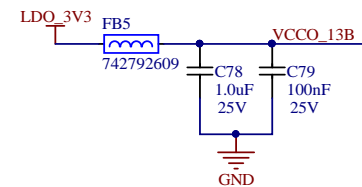
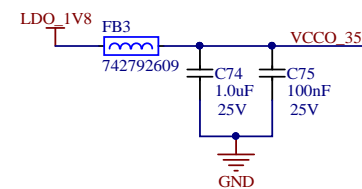
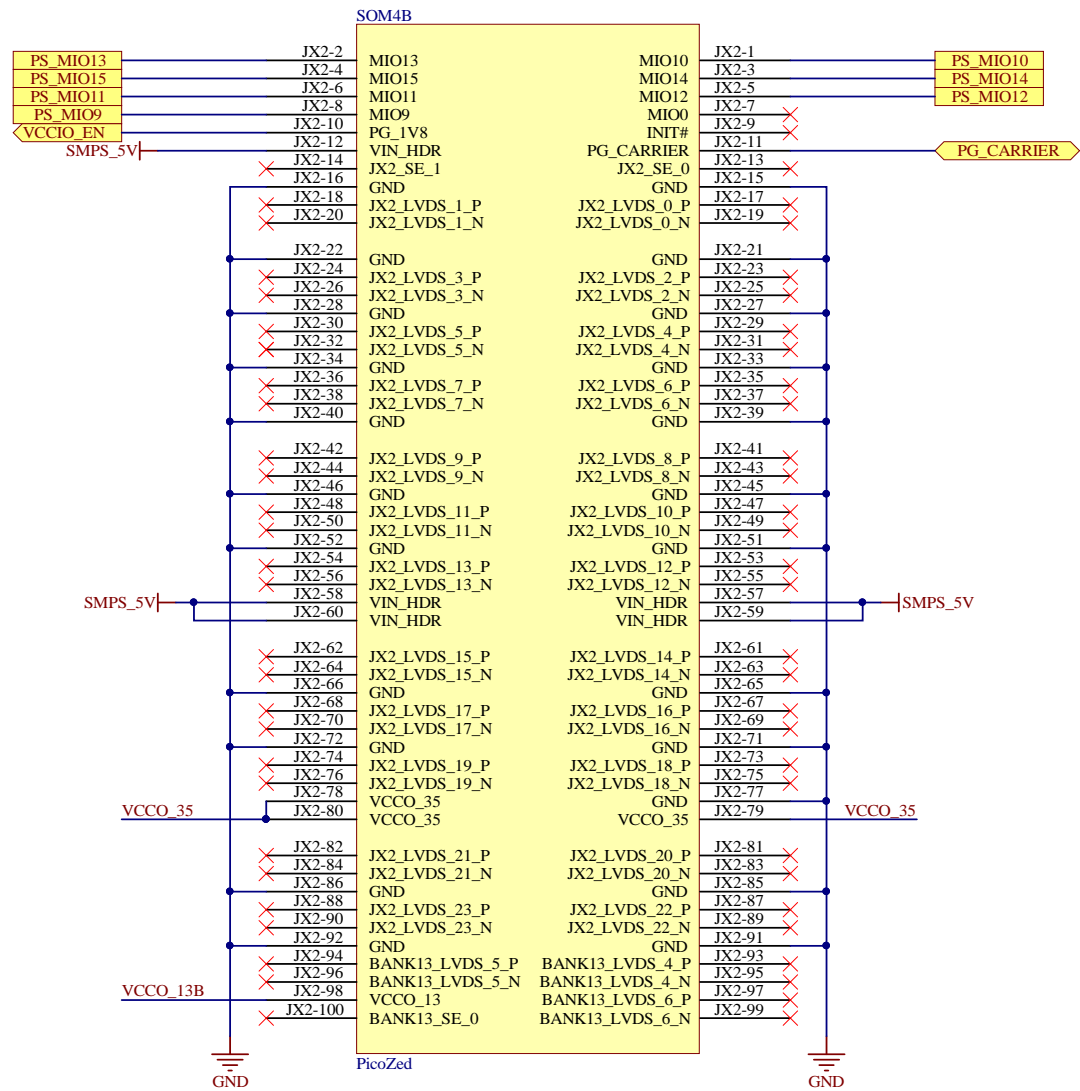


CMV\_OUT N[0..16]  
CMV\_OUT P[0..16]

		Title: PicoZed FPGA Part A	
		Project: HSI Prototype	Engineer: Julian V.
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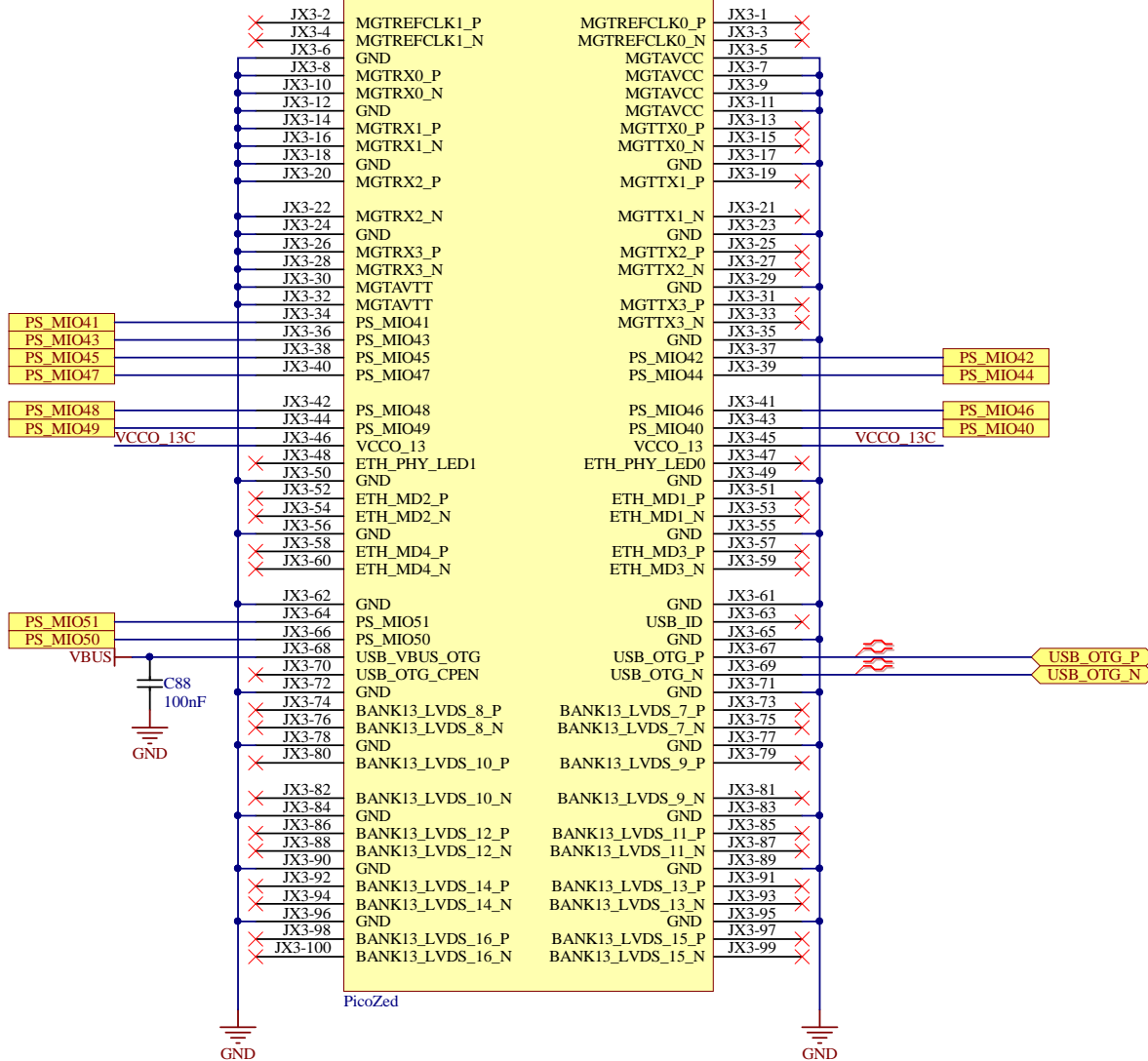
# ZYNQ BANK 34/35



	Title: PicoZed FPGA Part B		
	Project:	HSI Prototype	Engineer: Julian V.
	Pcb#	ML-002	Date: 11/01/2018
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# ZYNQ BANK 13, 501

SOM4C



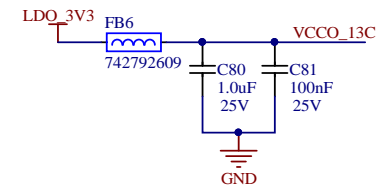
▲ USB Connector should be connected to:

- USB\_OTG\_N
- USB\_OTG\_P
- USB\_ID
- USB\_OTG\_CPEN

USB\_OTG\_CPEN signal allows the user to control an external power source for USB VBUS on the carrier board and is only used when USB operates in host mode.

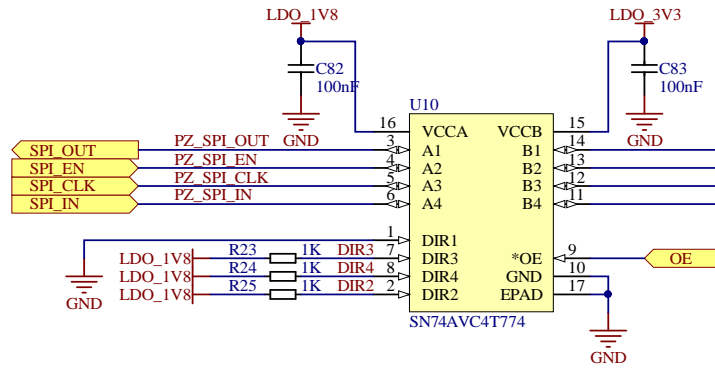
▲ JX3 connector used for microSD Card, UART, USB2.0 and bank 13 PL I/O

▲ SPI1 on MIO46 - MIO49  
UART0 on MIO50 - MIO51 (rx, tx)

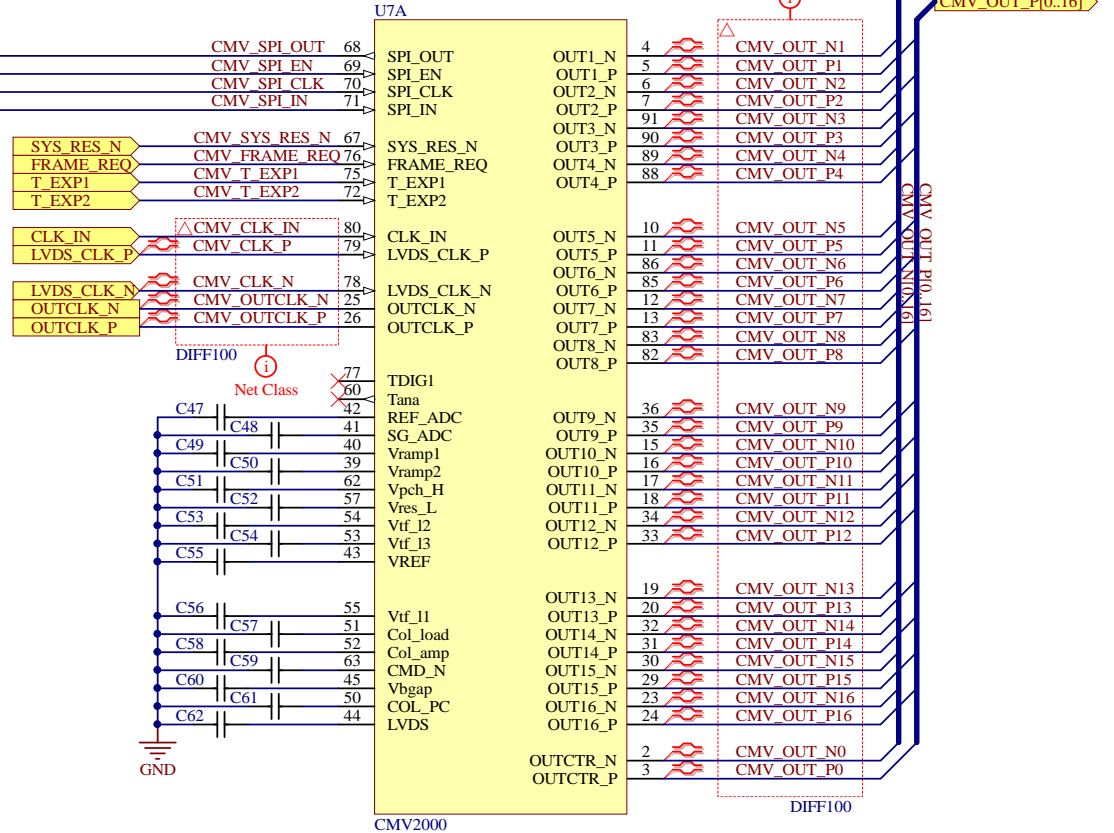


	Title: PicoZed FPGA Part C	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
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### Logic Level Converter



### Sensor Module



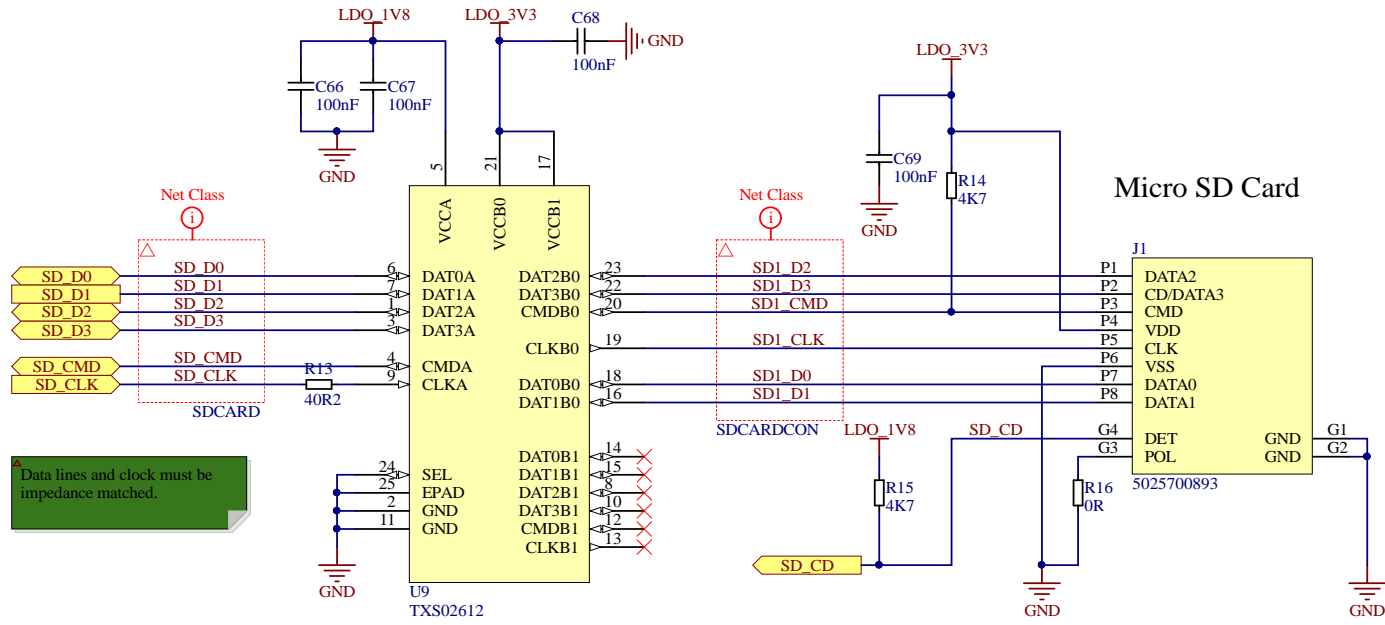
▲ CMV2000 Digital I/O operates on VDD33 logic high (minimum 2.0V) so level conversion is needed for the SPI bus.  
The control signals are routed to MIO0-15 signals on Bank501 which are already 3.3V logic high..

▲ SPI signals are connected to SPI on MIO46-MIO49 on Bank 501.  
See Zynq7000 technical specification page xx for complete MIO map.

	Title: CMOS Image Sensor	
	Project: HSI Prototype	Engineer: Julian V.
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The SD Card Interface is connected to SDIO0 on MIO 40-45 on Bank 501

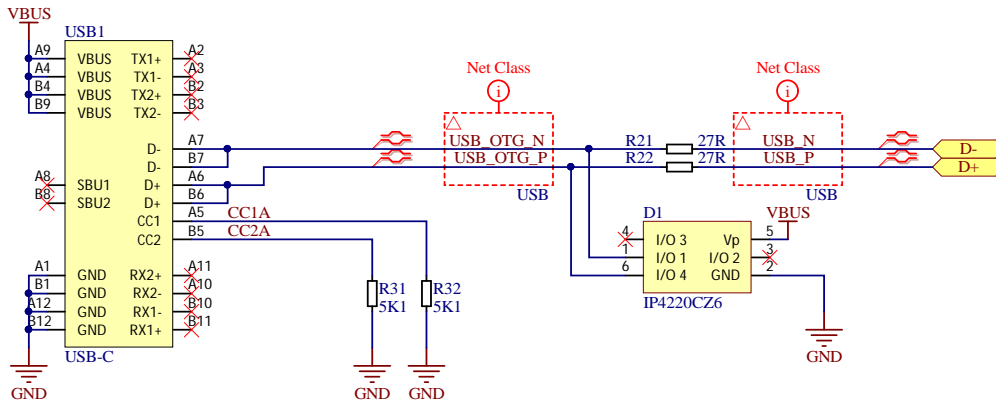
### Logic Level Translator



Data lines and clock must be impedance matched.

	Title: SD Card Interface	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
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## USB OTG Device

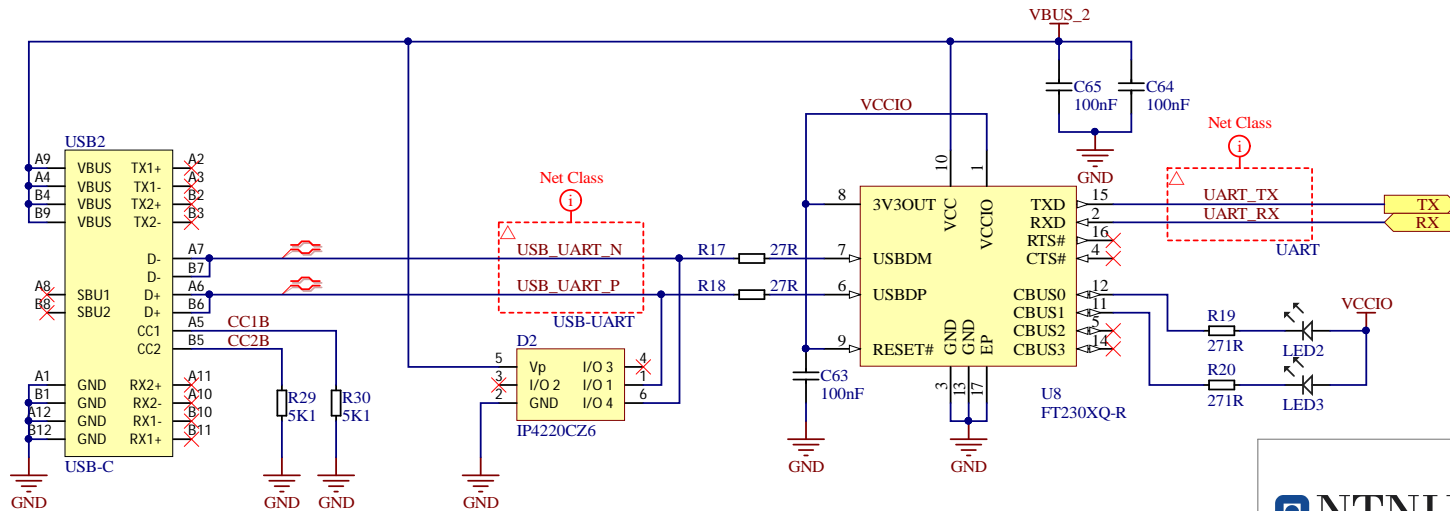


▲ UART is connected to UART0 MIO14-MIO15 on Bank 500.

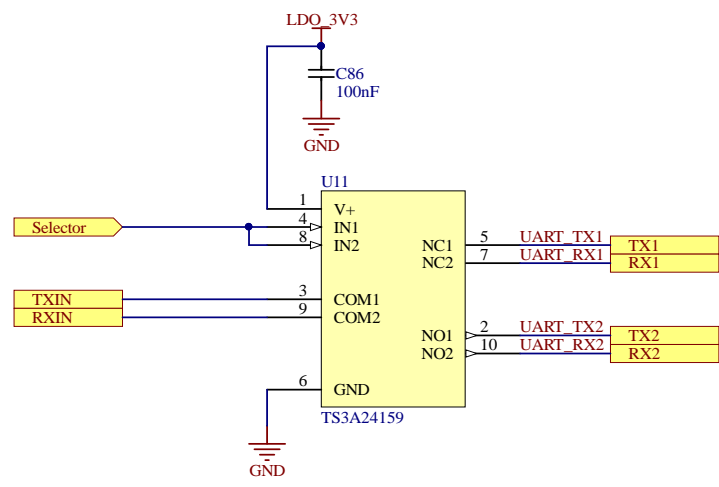
▲ The USB device is setup to act like a USB Device. See Chapter 15 of the Zynq7000 for USB implementation details.  
CPEN is not used (used to control external pwe supplies in Host mode). ID is left floating according to USB-B device standard.


▲ Add TUSB320 for USB-C CC role detection etc.  
IN UART C desing use two 5.1K pull down resistors on CC1 and CC2

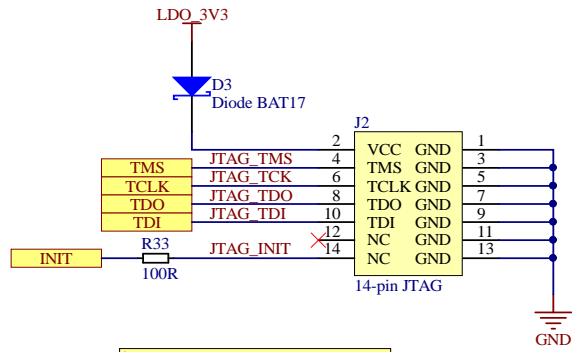
## USB UART BRIDGE



		Title: USB Manager	
		Project: HSI Prototype	Engineer: Julian V.
		Pcb#: ML-002	Date: 11/01/2018
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	Title: Digital UART Switch	
	Project: HSI Prototype	Engineer: Julian V.
	Pcb#: ML-002	Date: 11/01/2018
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**TODO:**

- Place BAT54LT1G zener diode in series with LDO\_3V3.
- Place R100 resistor in series with JTAG\_INIT
- Consider placing 74LCX125MTC

	Title: JTAG Interface	
	Project: HSI Prototype	Engineer: Julian V.
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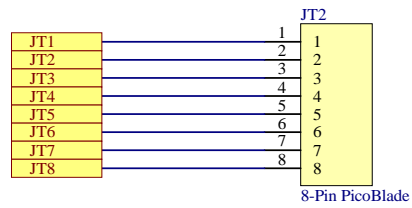
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	Title: External Connector	
	Project: HSI Prototype	Engineer: Julian V.
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