With the industrial version of the PicoZed Board this design is rated for -40 to 85 degrees celsius

With the industrial version of the PicoZed Board this design is rated for -40 to 85 degrees celsius

The camera can be powered by any power supply capable of delivering 4.5V - 14.5V at 6A

CARRIER_SRST# resets the processor as well as erases all debug configurations, memory content within the PS and PL.

To shut down power to the PicoZed, PWR_ENABLE and VCCIO_EN should be pulled low.

VCCIO_EN should be pulled low first to maintain proper shutdown sequencing.

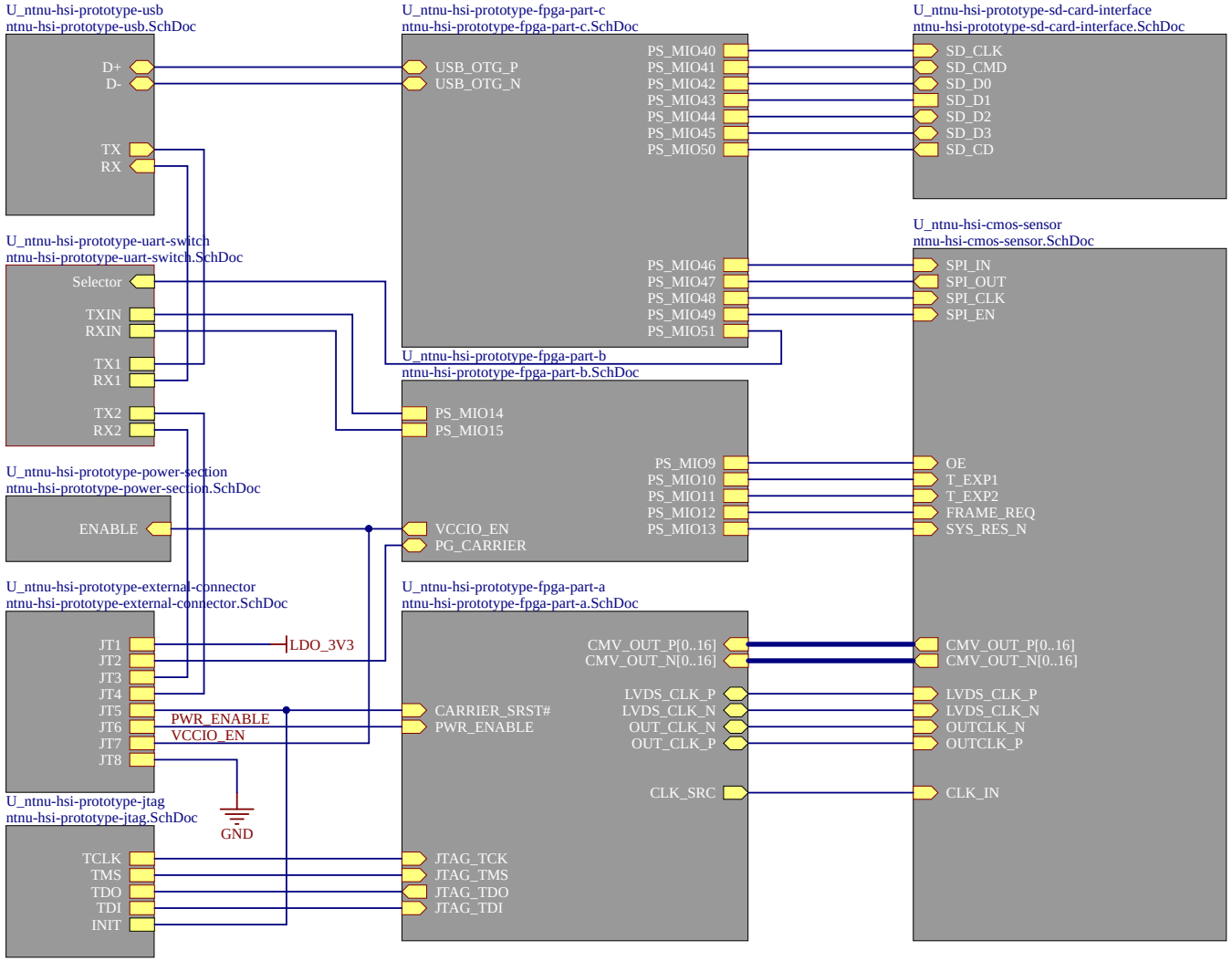
PWN_ENABLE is tied to VIN on the card

FPGA Bank 34 and 35 operate at 1.8V only because they are high-performance banks.

Bank 13 can be is 3.3V

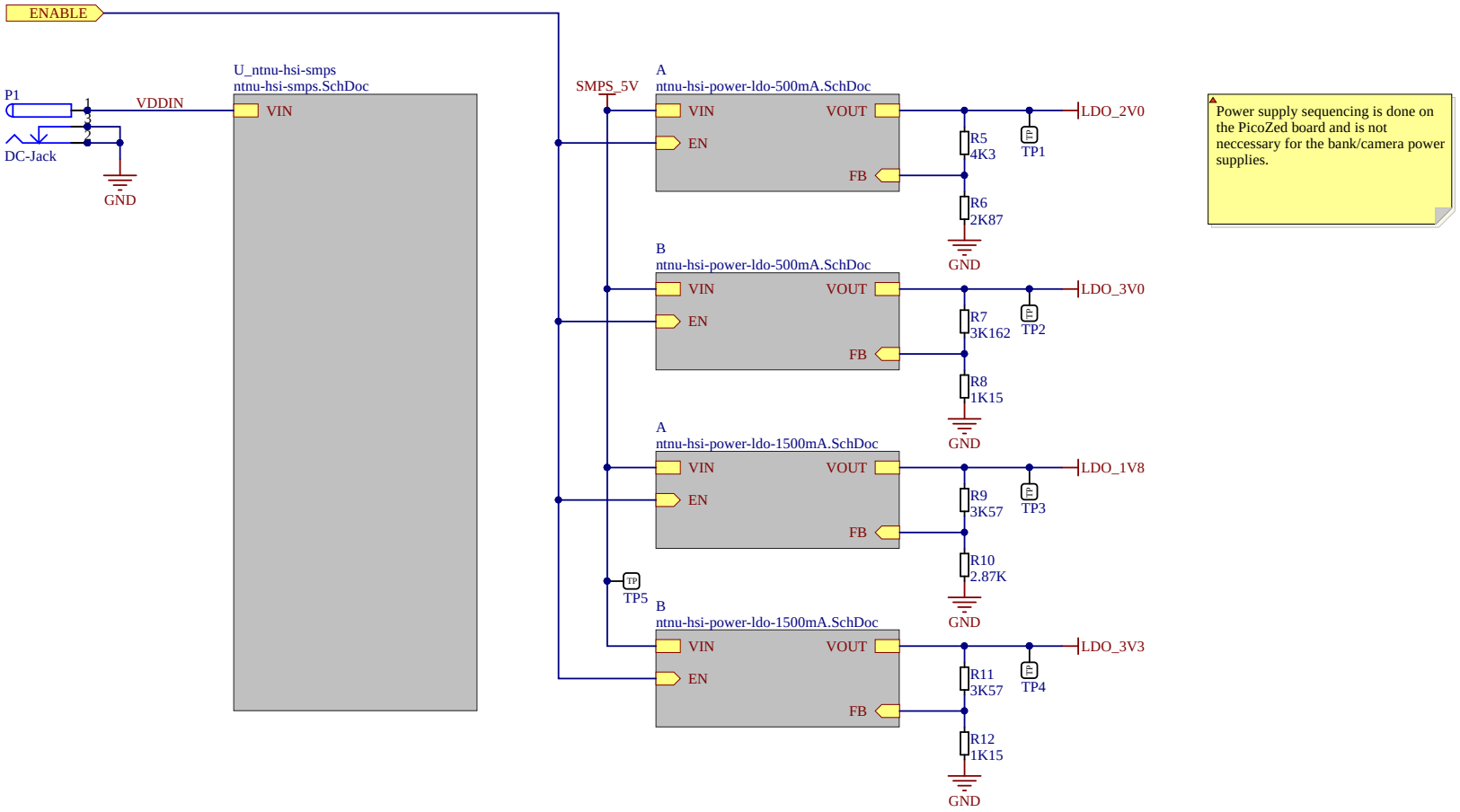
MIO0-MIO15 powered by 3.3V
MIO30-MIO51 powered by 1.8V

PG_MODULE - External power-on reset signal. Resets the entire chip



NTNU

Title:	Architecture Overview		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	1 of 15



Title:	Main Power Section		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	2 of 15

Vout = 5V
Rset = 196Ohm
Rt = 86.6kOhm
Switching frequency fsw: 780kHz

Undervoltage lockout at 5V:

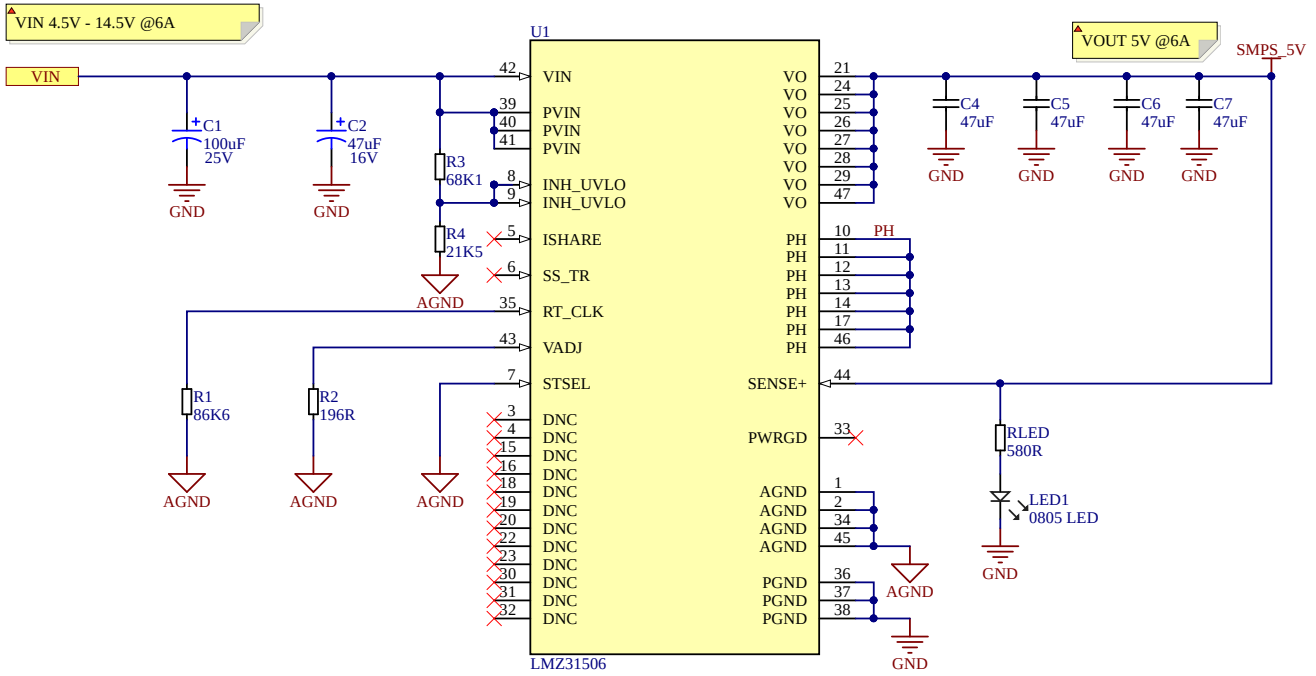
Ruvl1 = 68.1kOhm
Ruvl2 = 21.5kOhm

UVL Hysterisis: 400mV

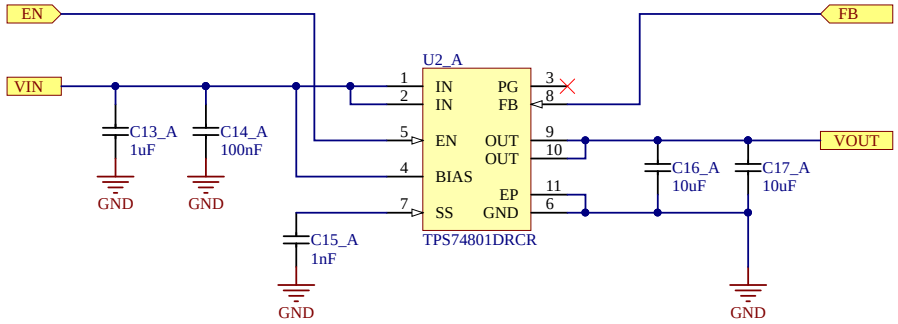
T525D476M016ATE035 16V 47uF

T521D107M025ATE040 25V 100uF

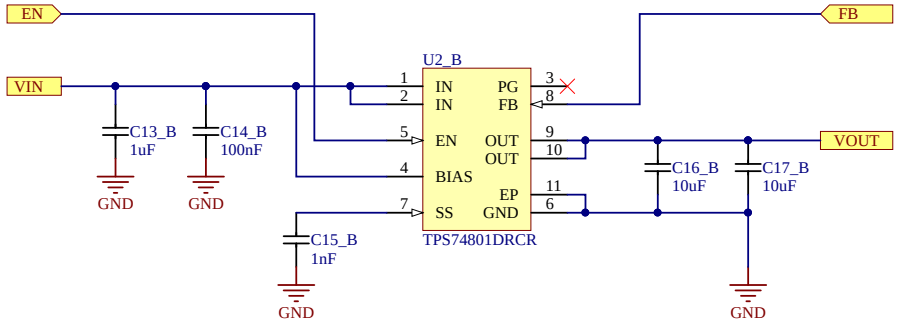
Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time.



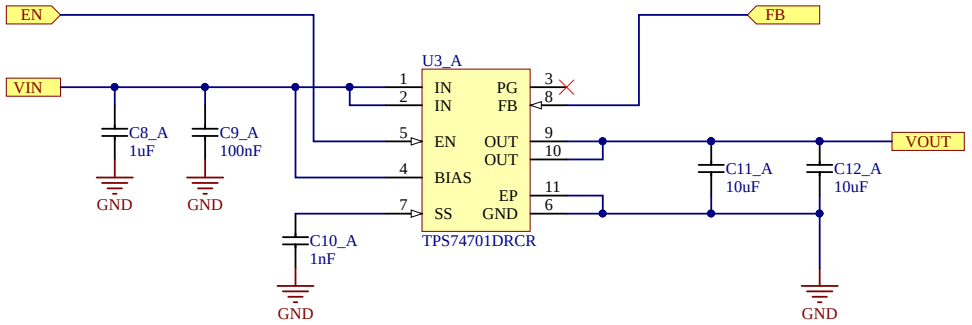
Title:	Switch Mode Power Supply		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	3 of 15



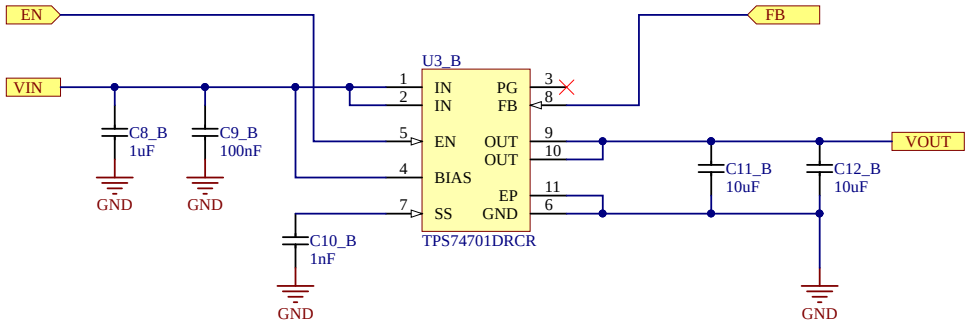
NTNU	Title:	1500mA Adjustable LDO	
	Project.	HSI Prototype	Engineer: Julian V.
	Pcb#	ML-002	Date: 19/01/2018
	Revision	1.0	Sheet 4 of 15



NTNU	Title:	1500mA Adjustable LDO	
	Project.	HSI Prototype	Engineer: Julian V.
	Pcb#	ML-002	Date: 19/01/2018
	Revision	1.0	Sheet 4 of 15

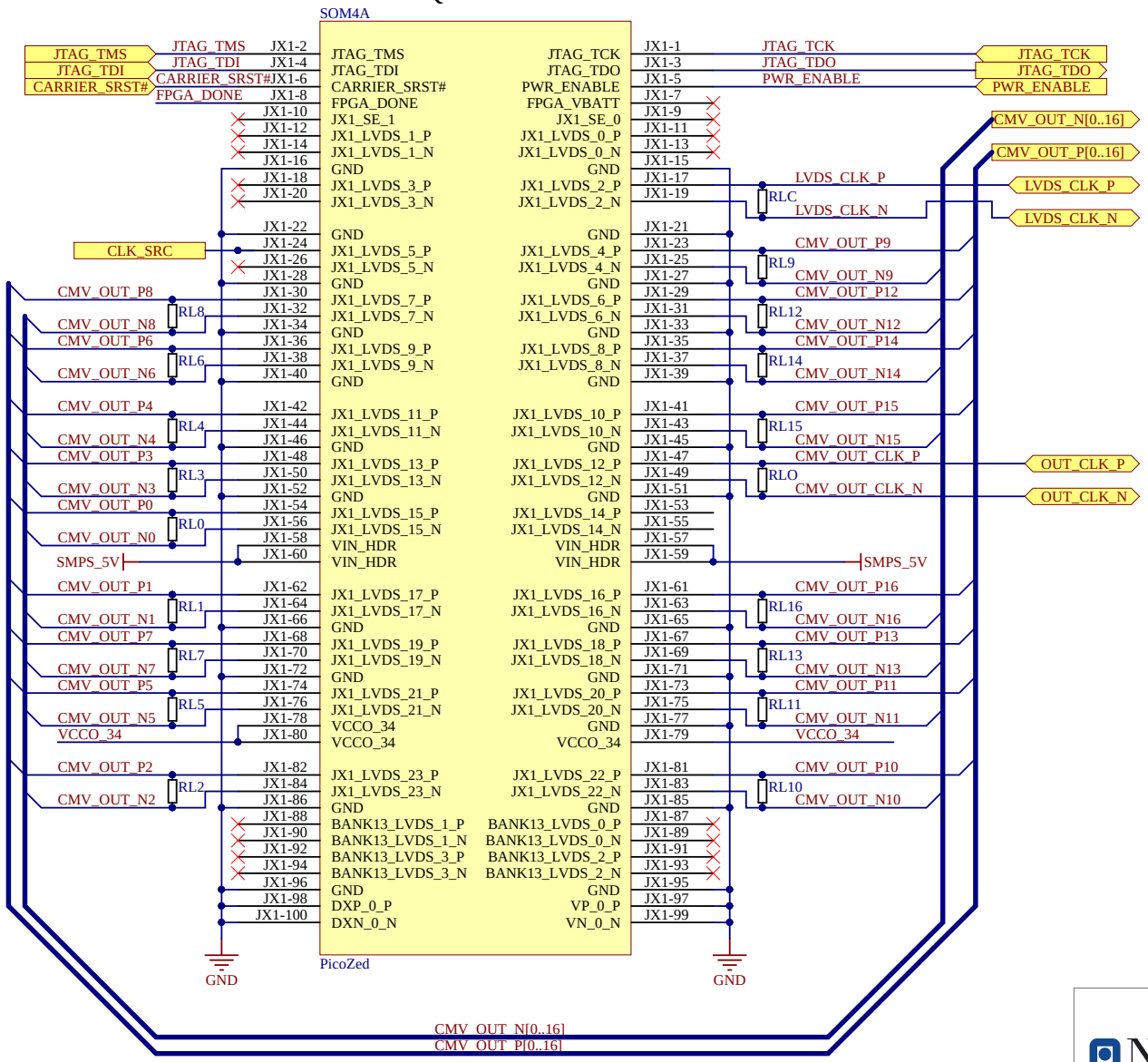


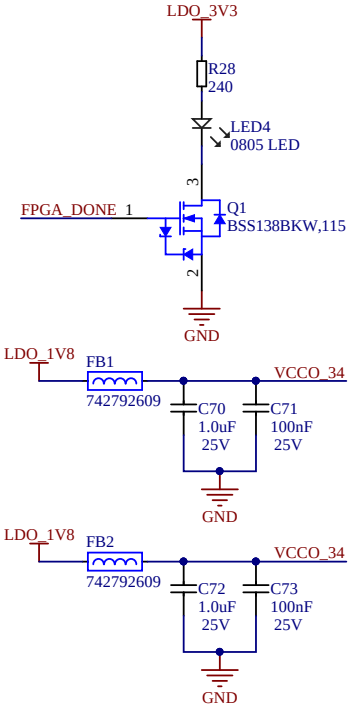
Title:	500mA Adjustable LDO		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	5 of 15



Title:	500mA Adjustable LDO		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	5 of 15

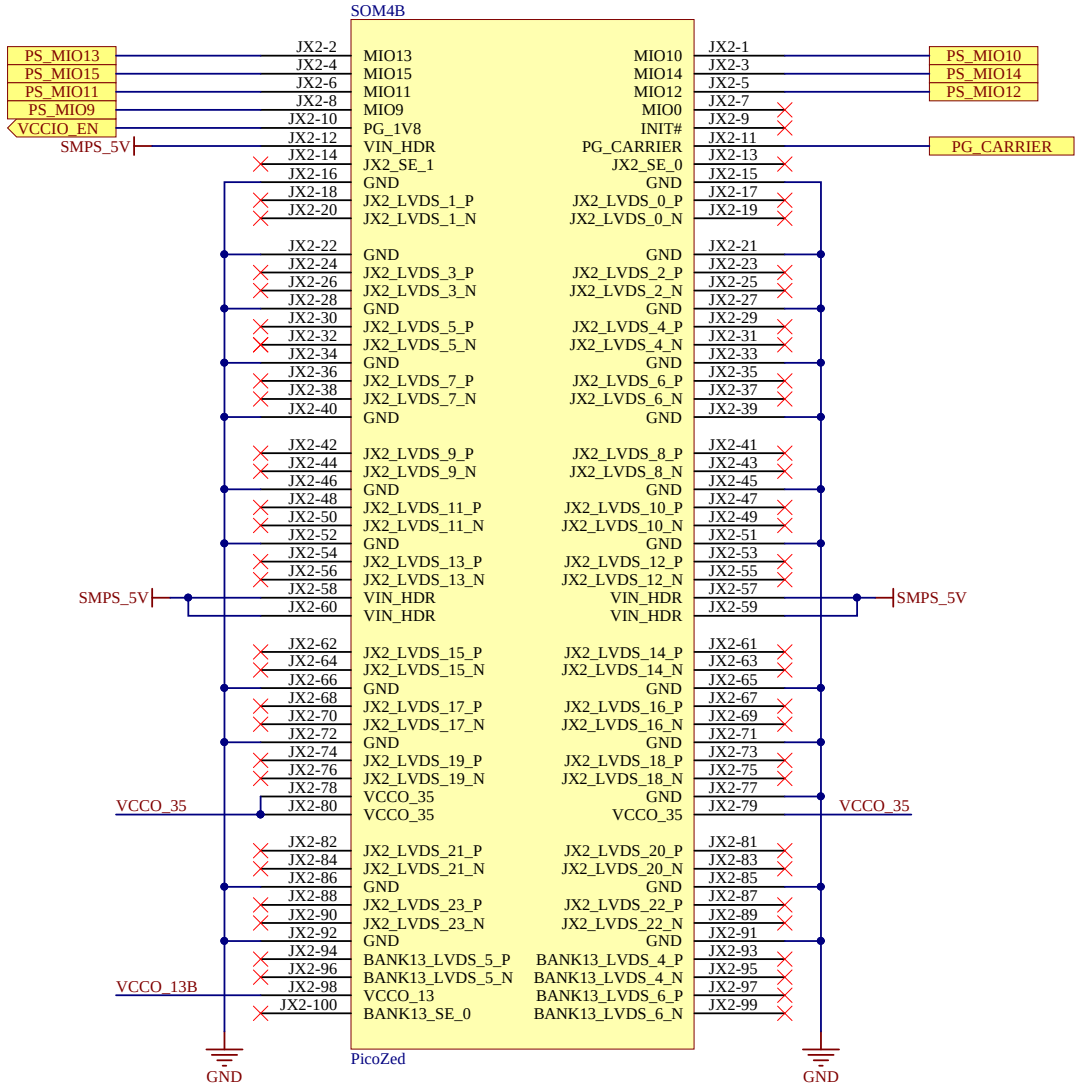
ZYNQ BANK 34/35

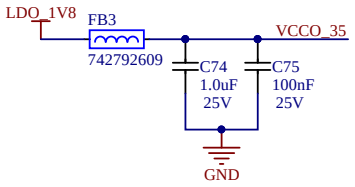


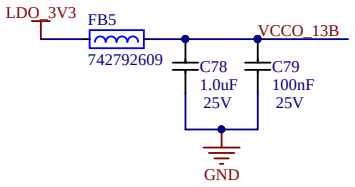


Title:	PicoZed FPGA Part A		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	6 of 15

ZYNQ BANK 34/35

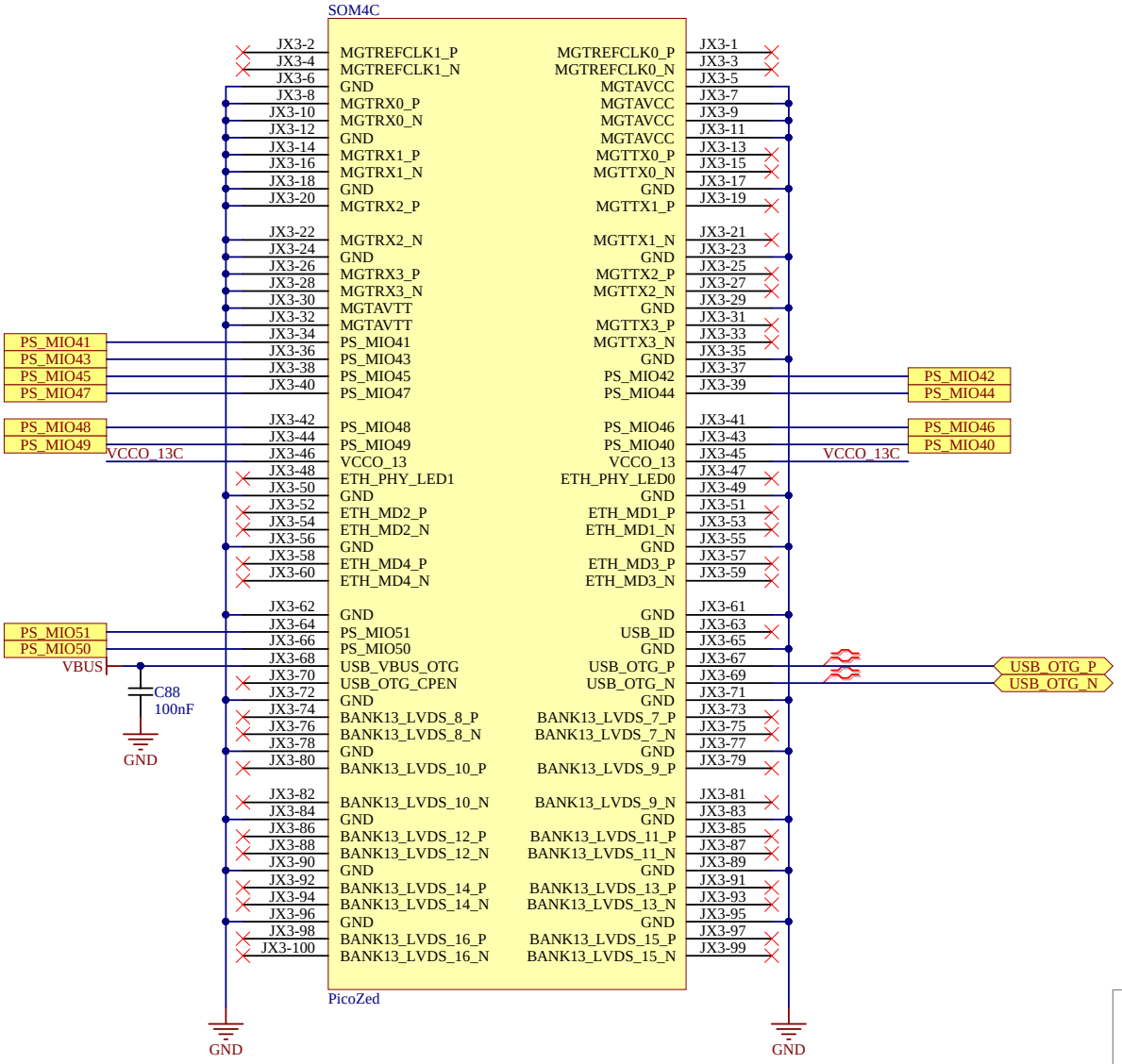






NTNU	Title:	PicoZed FPGA Part B	
	Project.	HSI Prototype	Engineer: Julian V.
	Pcb#	ML-002	Date: 19/01/2018
	Revision	1.0	Sheet 7 of 15

ZYNQ BANK 13, 501



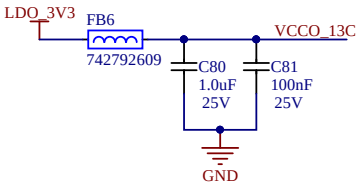
USB Connector should be connected to:

- USB_OTG_N
- USB_OTG_P
- USB_ID
- USB_OTG_CPEN

USB_OTG_CPEN signal allows the user to control an external power source for USB VBUS on the carrier board and is only used when USB operates in host mode.

JX3 connector used for microSD Card, UART, USB2.0 and bank 13 PL I/0

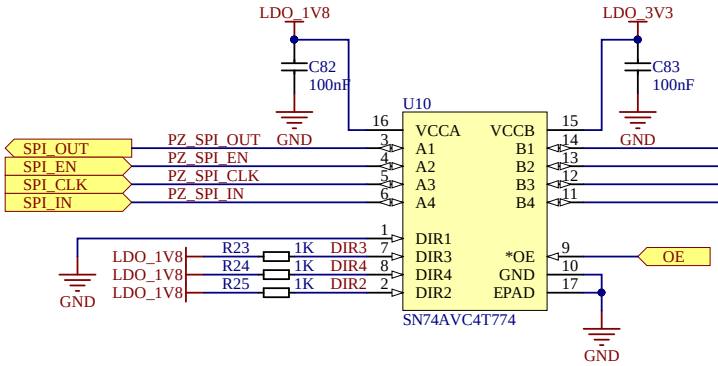
SPI1 on MIO46 - MIO49
UART0 on MIO50 - MIO51 (rx, tx)



NTNU

Title:	PicoZed FPGA Part C		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	8 of 15

Logic Level Converter



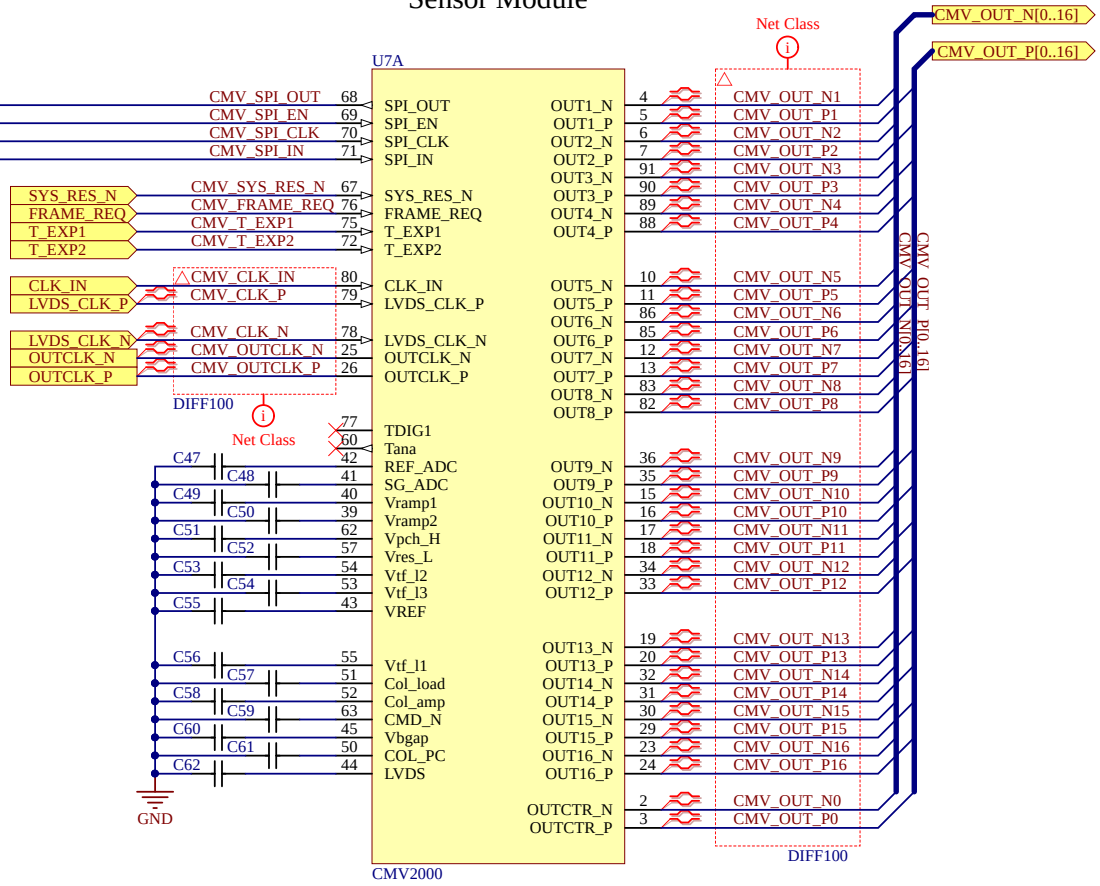
CMV2000 Digital I/O operates on VDD33 logic high (minimum 2.0V) so level conversion is needed for the SPI bus.

The control signals are routed to MIO0-15 signals on Bank501 which are already 3.3V logic high..

SPI signaks are connected to SPI on MIO46-MIO49 on Bank 501.

See Zynq7000 technical specification page xx for complete MIO map.

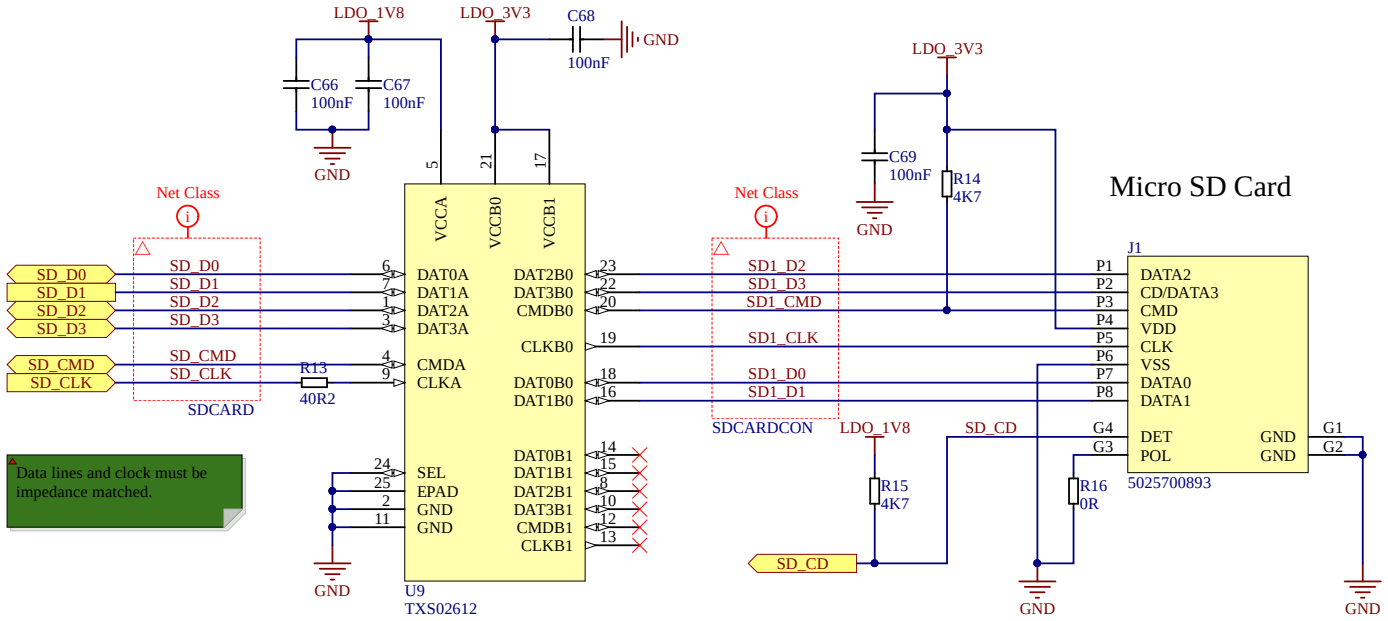
Sensor Module



Title:	CMOS Image Sensor		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	9 of 15

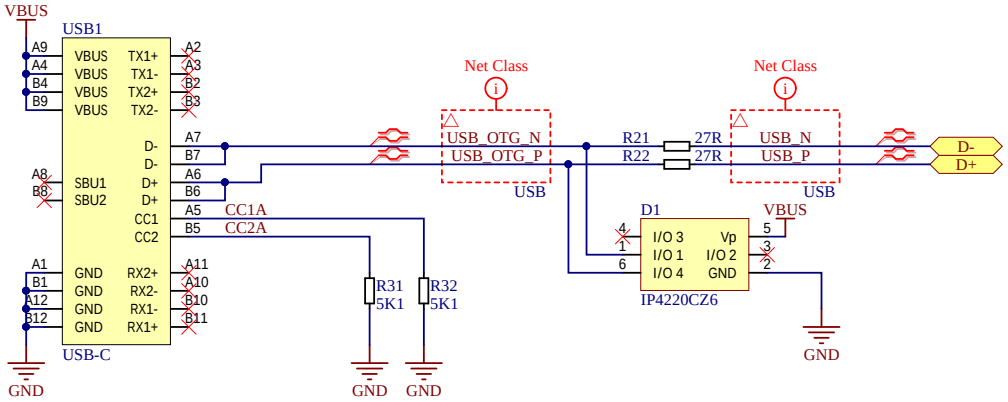
The SD Card Interface is connected to SDIO0 on MIO 40-45 on Bank 501

Logic Level Translator



Title:	SD Card Interface		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	11 of 15

USB OTG Device



UART is connected to UART0
MIO14-MIO15
on Bank 500.

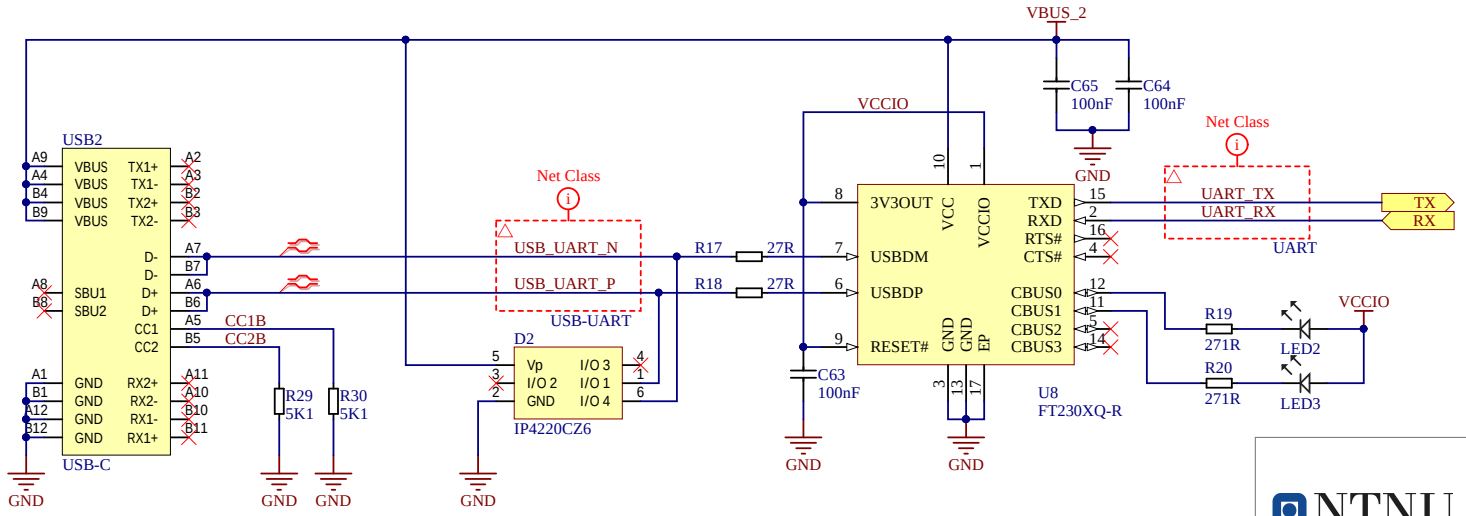
The USB device is setup to act like a USB Device. See Chapter 15 of the Zynq7000 for USB implementation details.

CPEN is not used (used to control external pwe supplies in Host mode). ID is left floating according to USB-B device standard.

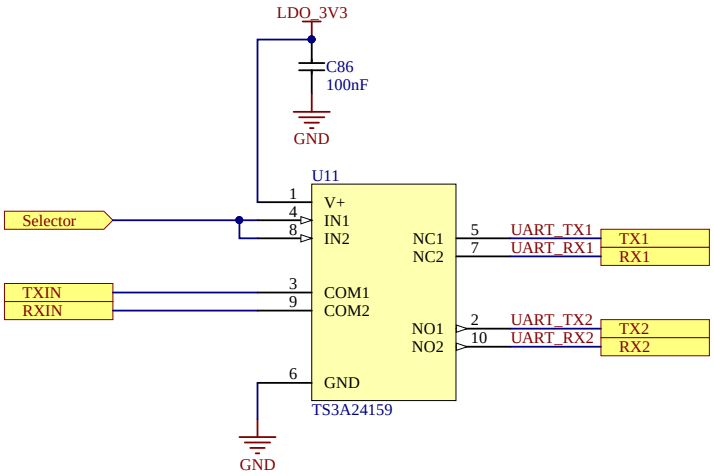
Add TUSB320 for USB-C CC role detection etc.

IN UART C desing use two 5.1K pull down resistors on CC1 and CC2

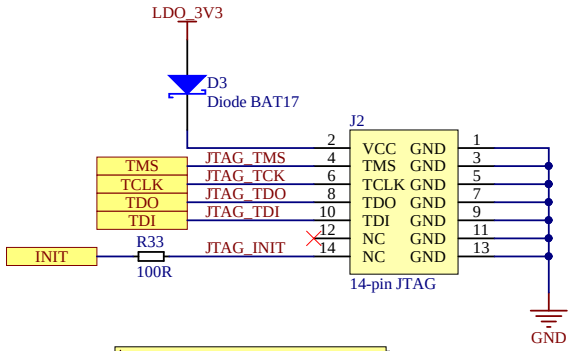
USB UART BRIDGE



Title:	USB Manager		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	12 of 15



NTNU	Title:	Digital UART Switch	
	Project.	HSI Prototype	Engineer: Julian V.
	Pcb#	ML-002	Date: 19/01/2018
	Revision	1.0	Sheet 13 of 15



TODO:

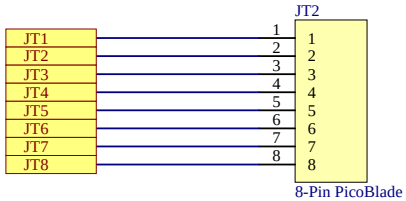
Place BAT54LT1G zener diode in series with LDO_3V3.

Place R100 resistor in series with JTAG_INIT

Consider placing 74LCX125MTC

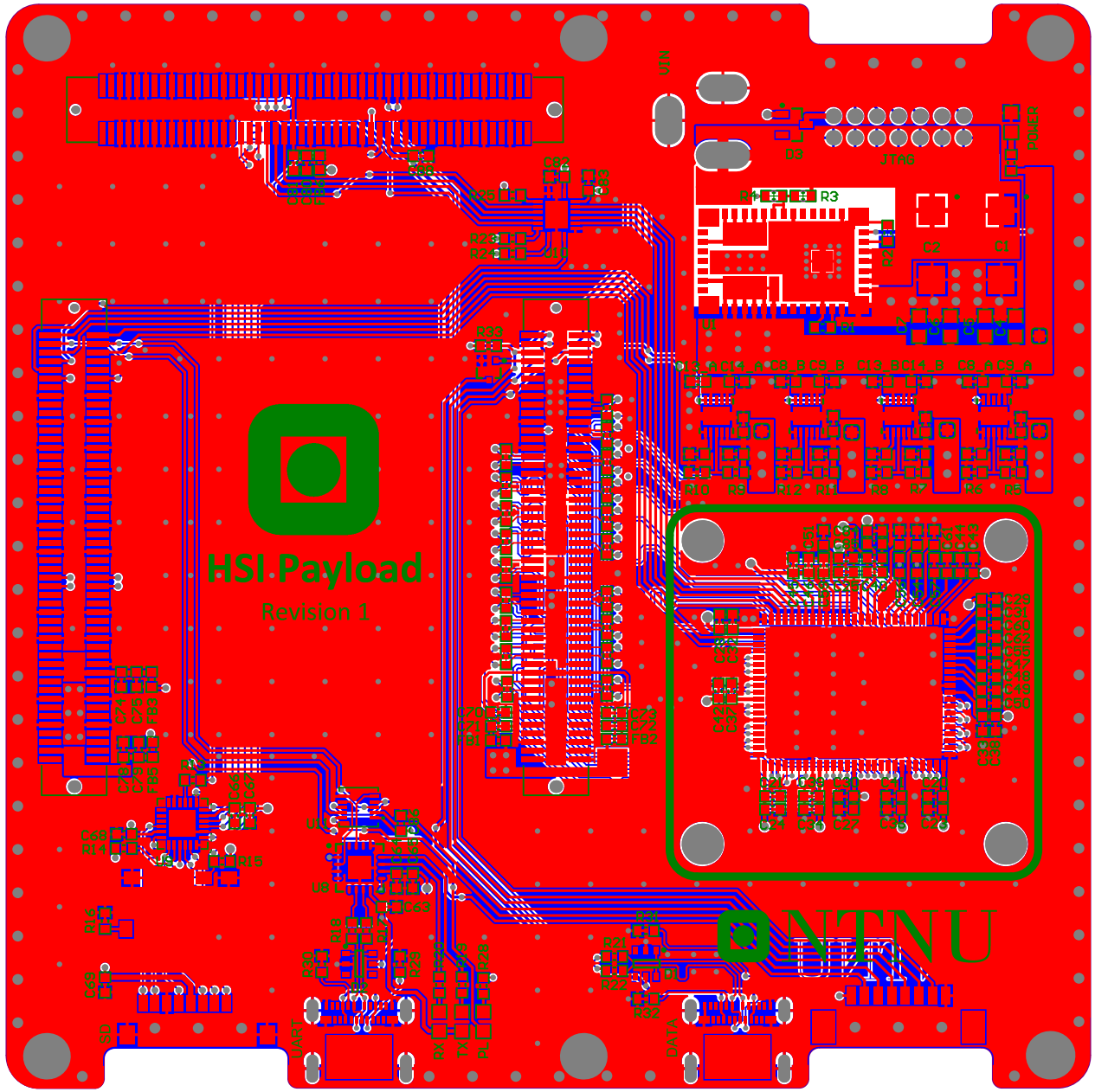
NTNU

Title:	JTAG Interface		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	14 of 15



NTNU

Title:	External Connector		
Project.	HSI Prototype	Engineer:	Julian V.
Pcb#	ML-002	Date:	19/01/2018
Revision	1.0	Sheet	15 of 15


HSI Payload
Revision 1
NTNU
JTAG
POWER
DATA
UART