

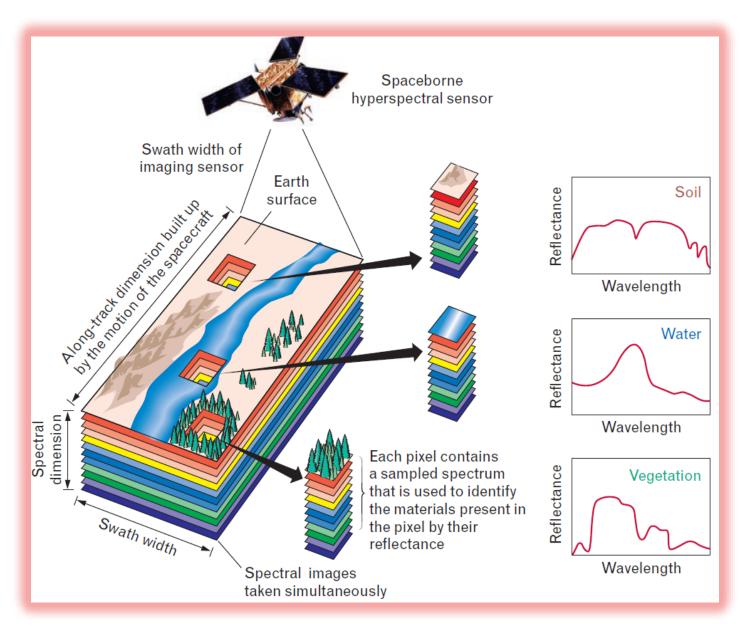
HSI payload software (FPGA)

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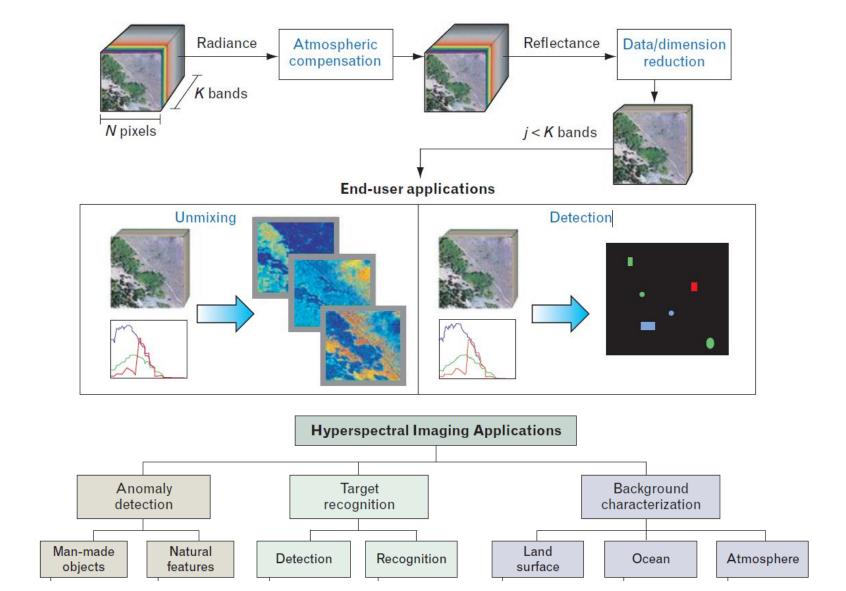


Introduction



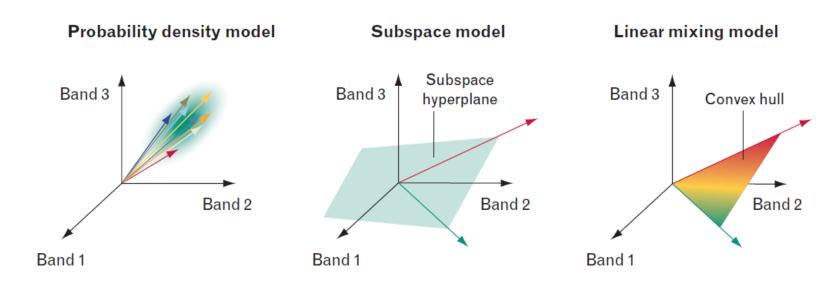


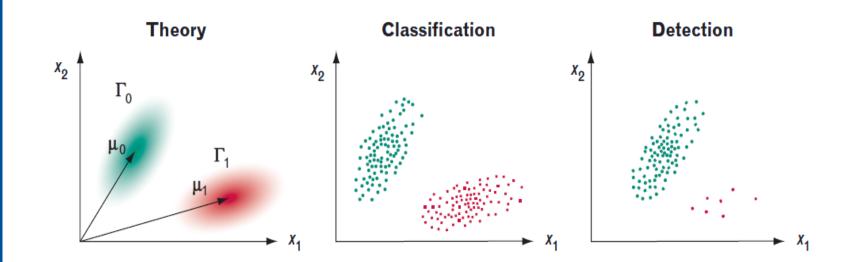
Dataflow in HSI processing





Spectral Variability Models







Target Detection

CEM, OSP

GLRT, ACE

AMSD, MF

Material
Count
Estimation
HFC VD
HySime

<u>Dimensionality</u>
<u>Reduction</u>
PCA,
MNF, ICA

<u>Anomaly Detection</u> Reed Xiaoli (RX) Endmember Finders ATGP, ICA-EEA, N-FINDR, VCA, PPI,

Least Square Solvers

FCLS NNLS

Spectral Comparison
SAM
SID
Normalized Cross Correlation



Taxonomy of Hyperspectral Imaging Target Detection Algorithms

Signal Model Ho:x - N(Po. Fo) A-priori information Target subspace Target abundance Background and noise covariance Background subspace and noise variance		Assumpti	ions D	$Petector y = D(\mathbf{x})$	Name	Comments	
		Κnowι μ ₀ , μ ₁ , Γ ₀		$(\mathbf{r} - \mathbf{\mu}_0)^T \mathbf{\Gamma}_0^{-1} (\mathbf{x} - \mathbf{\mu}_0) - (\mathbf{r} - \mathbf{\mu}_1)^T \mathbf{\Gamma}_1^{-1} (\mathbf{x} - \mathbf{\mu}_1)$	Bayes or Neyman- Pearson quadratio classifiers	$\Gamma \equiv \Gamma_1 = \Gamma_0 \Rightarrow$ $y = (\mu_1 - \mu_0)^T \Gamma^{-1} \mathbf{x}$ Plug-in detectors: estimate $\mu_1, \mu_0, \Gamma_1, \Gamma_0$	
		Quantity	Matched filt	ter Clairvoyant	Adaptive	Anomaly detection	
		S a T	Known Known Known	Known Unknown Known	Known Unknown Unknown	Unknown Unknown Unknown	
		$B, \sigma_{\rm w}^2$	Known	Known	Unknown	Unknown	
Su bpixel target:		P = 1 ⇒ S	\rightarrow s $(s^T \hat{\Gamma}$	$s^{T}\hat{\Gamma}^{-1}x$ $s^{1/2}(\psi_1 + \psi_2 x^{T}\hat{\Gamma}^{-1}x)^{1/2}$	estimator	$\Rightarrow \hat{\mathbf{\Gamma}}^{-1} = \sum_{k=1}^{Q} \frac{1}{\lambda_k} \mathbf{u}_k \mathbf{u}_k^T$	
Subpixe	H_0 : $\mathbf{x} = \mathbf{B}\mathbf{a}_{k,0} + \mathbf{w}$ H_1 : $\mathbf{x} = \mathbf{S}\mathbf{a} + \mathbf{B}\mathbf{a}_{k,1} + \mathbf{w}$	$\mathbf{w} \sim N(0, 0)$ $\mathbf{P}_A^{\perp} \equiv \mathbf{I} - \mathbf{A}(\mathbf{A}^2)$		$\frac{\mathbf{x}^T (P_B^\perp - P_{SB}^\perp) \mathbf{x}}{\mathbf{x}^T P_{SB}^\perp \mathbf{x}}$	GLRT detector	$SINR_{\alpha} = \frac{\left P_{\beta}^{\perp} S_{\mathbf{a}} \right ^{2}}{\sigma_{w}^{2}}$	



FPGA Implementation of the N-FINDR Algorithm for Remotely Sensed Hyperspectral Image Analysis

Carlos González, Daniel Mozos, Javier Resano, and Antonio Plaza, Senior Member, IEEE

IEEE JOURNAL OF SELECTED TOPICS IN APPLIED EARTH OBSERVATIONS AND REMOTE SENSING, VOL. 8, NO. 6, JUNE 2015

Dual-Mode FPGA Implementation of Target and Anomaly Detection Algorithms for Real-Time Hyperspectral Imaging

Bin Yang, Minhua Yang, Antonio Plaza, Fellow, IEEE, Lianru Gao, Member, IEEE, and Bing Zhang, Senior Member, IEEE

DBSERVATIONS AND REMOTE SENSING, VOL. 8, NO. 6, JUNE 2015

J Real-Time Image Proc DOI 10.1007/s11554-016-0650-7

ORIGINAL RESEARCH PAPER

FPGA implementation of the principal component analysis algorithm for dimensionality reduction of hyperspectral image

Daniel Fernandez¹ · Carlos Gonzalez¹ · Daniel Mozos¹ · Sebastian Lopez²

Received: 17 May 2016 / Accepted: 24 October 2016

fpga Implementation of the HySime Algorithm for the Determination of the Number of Endmembers in Hyperspectral Data

Carlos Gonzalez, Sebastian Lopez, Senior Member, IEEE, Daniel Mozos, and Roberto Sarmiento

IEEE JOURNAL OF SELECTED TOPICS IN APPLIED EARTH OBSERVATIONS AND REMOTE SENSING, VOL. 9, NO. 9, SEPTEMBER 2016

FPGA Implementation of an Algorithm for Automatically Detecting Targets in Remotely Sensed Hyperspectral Images

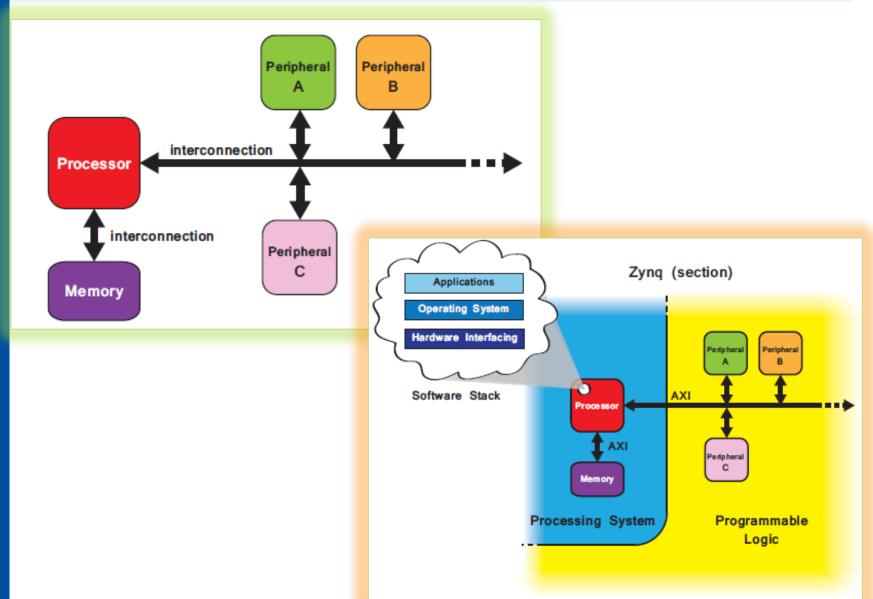
Carlos González, Sergio Bernabé, Daniel Mozos, and Antonio Plaza

Abstract—Timely detection of targets continues to be a relevant allenge for hyperspectral remote sensing capability. The tomatic target-generation process using an orthogonal projectn operator (ATGP-OSP) has been widely used for this pur-

Propulsion Laboratory in California, which developed instruments such as the airborne imaging spectrometer, then called airborne visible infrared imaging spectrometer (AVIRIS) [2].

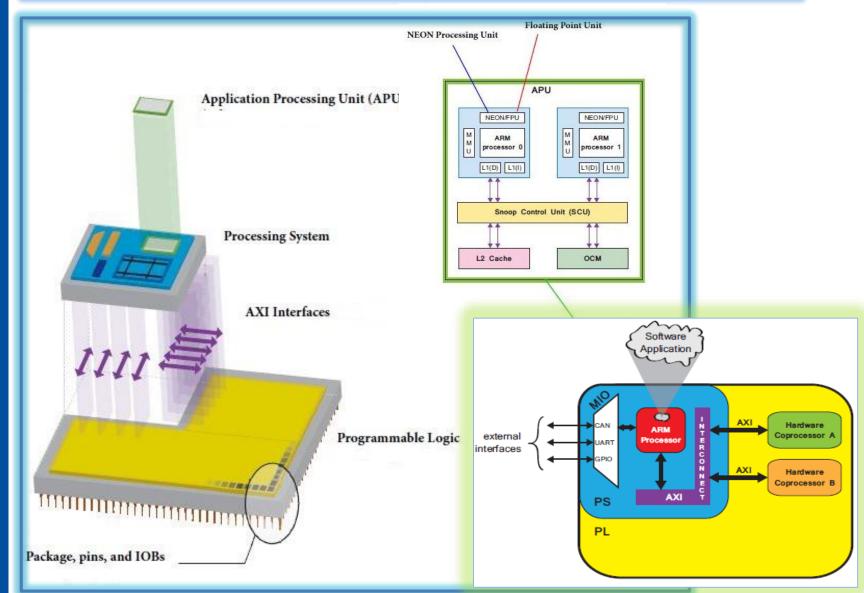


System architecture



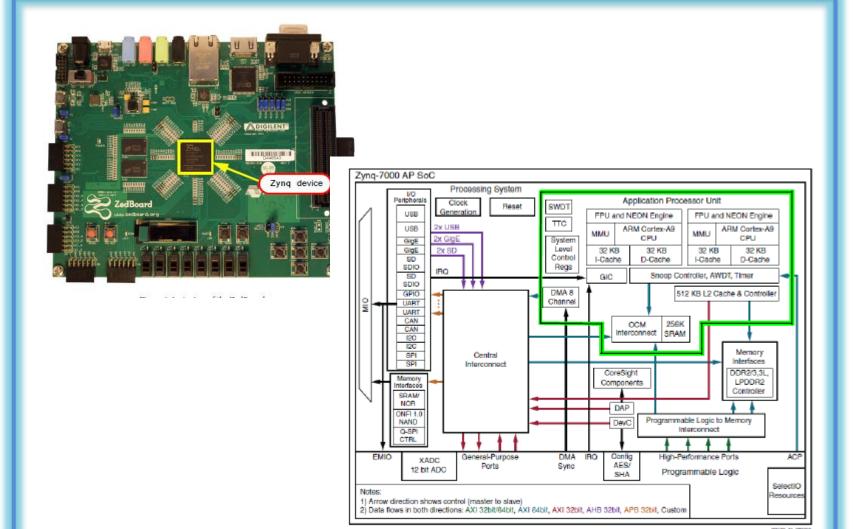


System Architecture (Zynq)





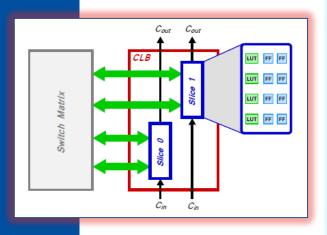
D Zynq Devices

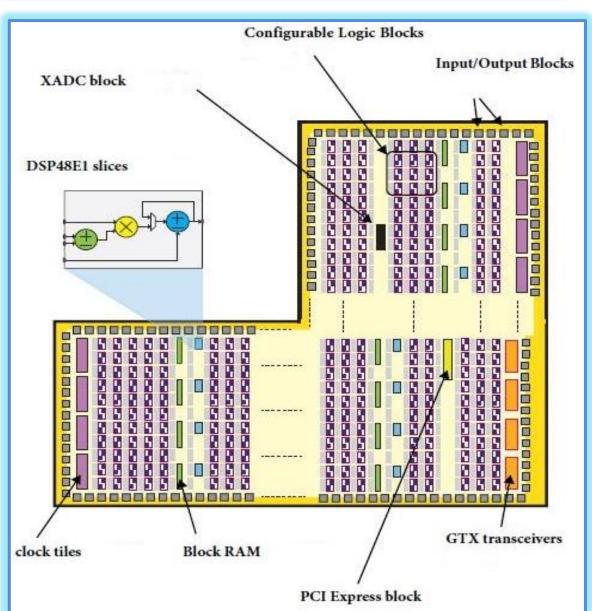


@ Xilinx



Programmable Logic







Zyna-7000 All Programmable Soc

	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
,	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
le Logic	Block RAM (# 36 Kb Blocks)	1.8 Mb (50)	2.5 Mb (72)	3.8 Mb (107)	2.1 Mb (60)	3.3 Mb (95)	4.9 Mb (140)	9.3 Mb (265)	17.6 Mb (500)	19.2 Mb (545)	26.5 Mb (755)
Programmable	DSP Slices (18x25 MACCs)	66	120	170	80	160	220	400	900	900	2,020
Progra	Peak DSP Performance (Symmetric FIR)	73 GMACs	131 GMACs	187 GMACs	100 GMACs	200 GMACs	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express (Root Complex or Endpoint) ⁽³⁾		Gen2 x4			Gen2 x4		Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security ⁽²⁾	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication									



Why FPGA?

PRO:

- Compact SIZE
- · LOW WEIGHT
- LOWER POWER CONSUMPTION

(Xilinx 7 series)

- RECONFIGURABILITY (PARTIAL OR FULL)
- · HIGH THROUGHPUT
- REAL-TIME PROCESSING
- OPTIMIZED DATA PATHS
- RESISTS HIGH LEVEL RADIATION without changing the content of inner memories.

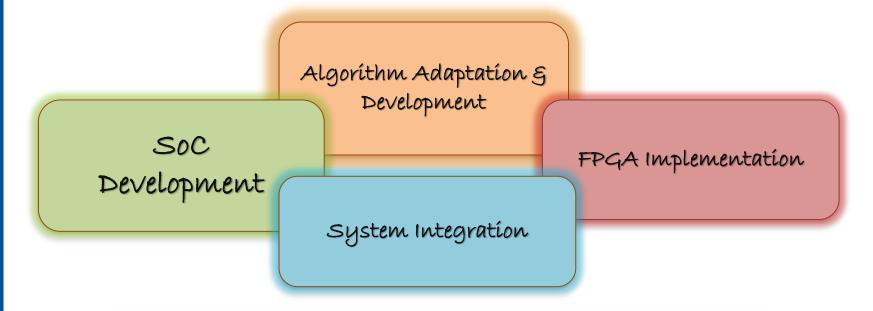
CONS:

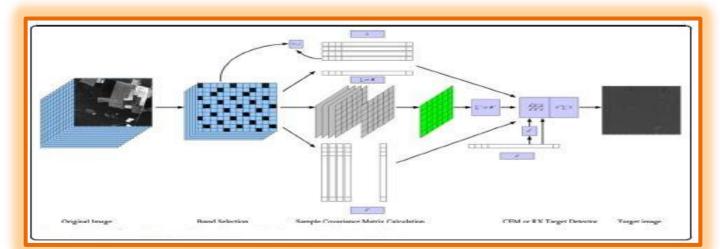
LOW LEVEL HDL LANGUAGES

Deep understanding OF HARDWARE DESIGN required



Challenges in HSI onboard system development







FPGA Implementation of OTFP Preprocessing Module (1/11)

SPECIFICATION:

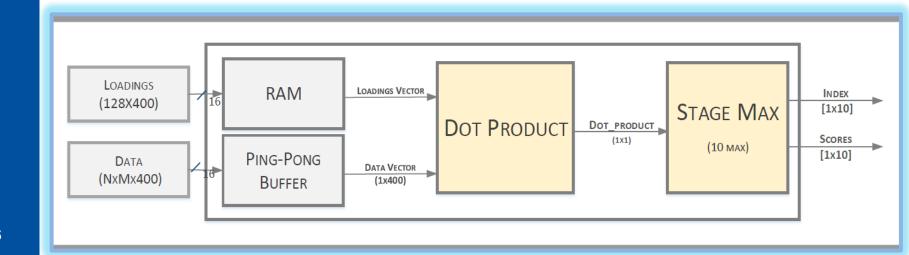
DATA CUBE- X (500x500x400)

N_load=128

Loadings_database= L(128x400)

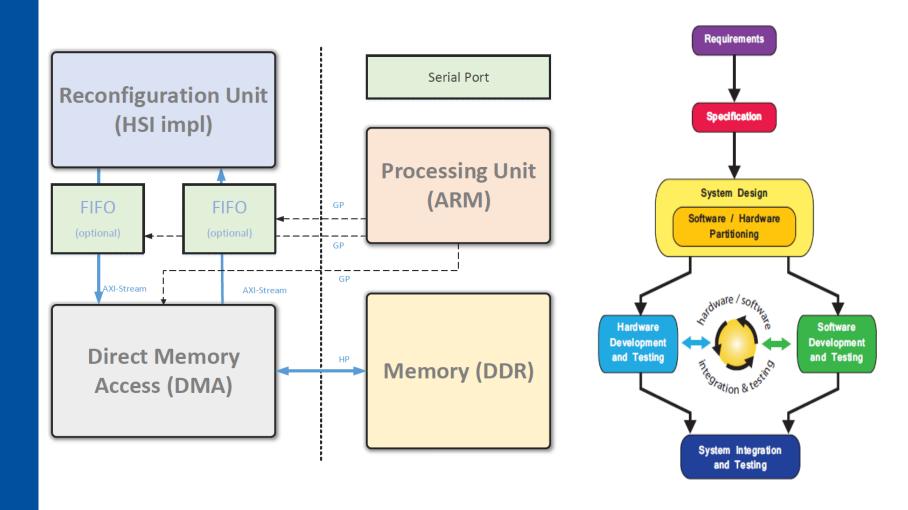
K_max=10

Preprocessing stage: $S = \sum L_i, k^* (X_i, j-X_mean[i])$ Scores = max(S, k max)





Soc Development and System Intergration for HSI application





Dynamic Partial Reconfiguration (DPR) Concept

